SPD5108/SPD5118

Serial Presence Detect (SPD) EEPROMs

Description

The SPD5 Hub device family contains 1024 bytes of non-volatile memory arranged as 16 blocks of 64 bytes per block. Each block may optionally be write protected via software command. Write protection for each block may be overridden in an offline programmer environment while overrides are prevented in normal use. The SPD5 Hub device operate from a single 1.8V nominal power supply. The SPD5 device is intended to operate up to 12.5MHz on a 1.0V to 1.2V or 1.8V I3C Basic IO bus or up to 1MHz on a 1.0V to 3.3V I^2C IO bus. The SPD5 devices are intended to interface to I^2C/I3C Basic buses which have multiple devices on a shared bus, and must be uniquely addressed with fixed addressing on the same bus.

All SPD5 Hub devices respond to specific pre-defined I^2C/I3C Basic device select codes on a host interface bus. The SPD5118 and SPD5108 devices also incorporate a second local I^2C/I3C Basic bus and support pass through of commands from the host bus onto the local bus for addressing of I^2C/I3C Basic devices on the local bus (Hub function).

The SPD5118 incorporates a thermal sensing capability that is controlled and read over the I2C/I3C Basic bus. The SPD5108 device supports the same functionality as the SPD5118 but without the thermal sensing function.

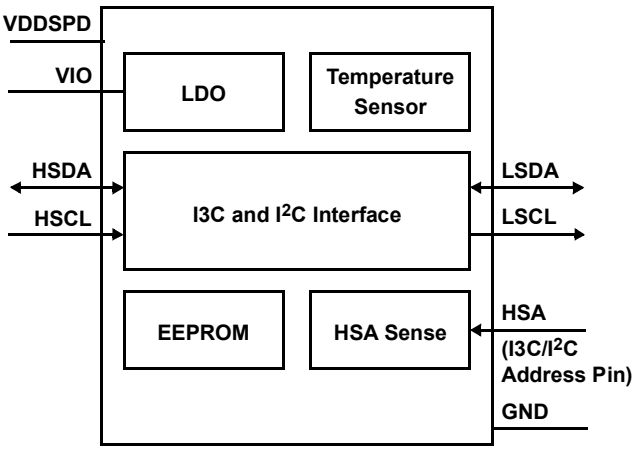


Figure 1. SPD5118 Block Diagram

Features

- SPD5 Hub Device
- Two-wire programmable I^2C or I3C Basic bus serial interface
- Single device load on the Host bus
- Up to 12.5MHz transfer rate
- 1.8V power supply input
- 1.0V LDO output at VIO pin; Optionally can take 1.0V input power supply on VIO pin
- Supports 1.0V, 1.1V, 1.2V, and 1.8V Push-Pull IO levels
- Supports 1.0V, 1.1V, 1.2V, 1.8V, 2.5V, and 3.3V Open-drain IO levels
- 16 blocks of non-volatile memory; 64 bytes per block
- Hub Function (a.k.a. Transparent Mode of operation) with 3 address bit translation
- Integrated Temperature Sensor; 0.5°C Accuracy with 0.25°C resolution
- Packet Error Check (PEC) Function
- Parity Error Check Function
- Bus Reset Function
- Up to 8 unique addressing
- Programmable I^2C, I3C Basic Bus Addressing Scheme
- In Band Interrupt (IBI) (Transparent Mode of Operation)
- Write protection for each block of NVM
- 9-pin thermally enhanced DFN package
- Temperature: Industrial range of -40°C to 125°C

Table 1. Device Part Numbers and Feature Summary

Part Number	Hub Function	Internal Thermal Sensor	Non Volatile Memory (Bytes)	I^2C/I3C Basic Address (xxx = 000 to 111)
SPD5118	Yes	Yes	1024	101 0xxx
SPD5108	Yes	No	1024	101 0xxx

Contents

1. Pin Information

1.1 Pin Assignments

The SPD5 device is packaged in a 9-contact thermally enhanced PSON-8, MO-229 var V/W/UCED-3. The package size is 2.0mm x 3.0mm. The DFN package pinouts for SPD5118 and SPD5108 are shown in Figure 2. The pinouts are bottom view.

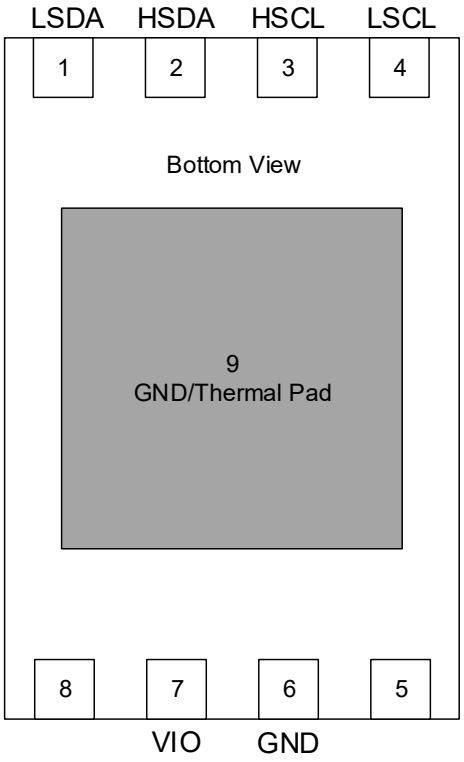


Figure 2. 9 Pin Thermally Enhanced DFN Package Pinouts - Bottom View

1.2 Pin Descriptions

Table 2. Pin Description

Pin #	Pin Name	Pin Type	Description
5	VDDSPD	Power	1.8V Input Power Supply
6	VSS	GND	GND
3	HSCL	I	Host Bus - I^2C/I3C Basic Input Clock
2	HSDA	IO	Host Bus - I^2C/I3C Basic Data
8	HSA	I	Host Bus - I^2C/I3C Basic Address Pin. See Table 98 for ID definition.
4	LSCL/RFU	O	Local Bus - I^2C/I3C Basic Output Clock
1	LSDA/RFU	IO	LSDA - Local Bus - I^2C/I3C Basic Data
7	VIO	I/Power	Connect minimum of 1.0µF capacitor for 1.0V LDO output to filter the noise. This pin can also take external 1.0V Power Supply Input in which case internal 1.0V LDO is not used. External capacitor must be still present.
9	Thermal Pad, GND	GND	Connected to GND Plane

1.2.1 Pin Definitions

Table 3. Pin Definitions

Pin #	Pin Name	Pin Type	SPD 5118	SPD 5108
5	VDDSPD	Power	Yes	Yes
6	VSS	GND	Yes	Yes
3	HSCL	I	Yes	Yes
2	HSDA	IO	Yes	Yes
8	HSA	I	Yes	Yes
4	LSCL/RFU	O	LSCL	LSCL
1	LSDA/RFU	IO	LSDA	LSDA
7	VIO	I/Power	Yes	Yes
9	Thermal Pad, GND	GND	Yes	Yes

2. Definition of SPD5118/5108 Hub Devices

2.1 Device Standard

This standard defines the specifications of interface parameters, signaling protocols, and features for Serial Presence Detect (SPD) EEPROM or other non-volatile memory technology (EE) and Temperature Sensor (TS) as used for memory module applications. Some devices include a Hub feature, allowing isolation of a local bus from a master host bus. The designations are SPD5118 and SPD5108.

The purpose is to provide a standard for the SPD5 family of devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

A single specification document for SPD5 family device is written to establish and maintain the commonality of these devices and promote the interchangeability of devices in target applications that may require the EE and TS for some uses and EE only for other uses.

The designations SPD5118 and SPD5108 refer to the part of the part designation of a series of commercial logic parts common in the industry.

2.2 Device Functional Diagram

2.2.1 SPD5 Hub Device

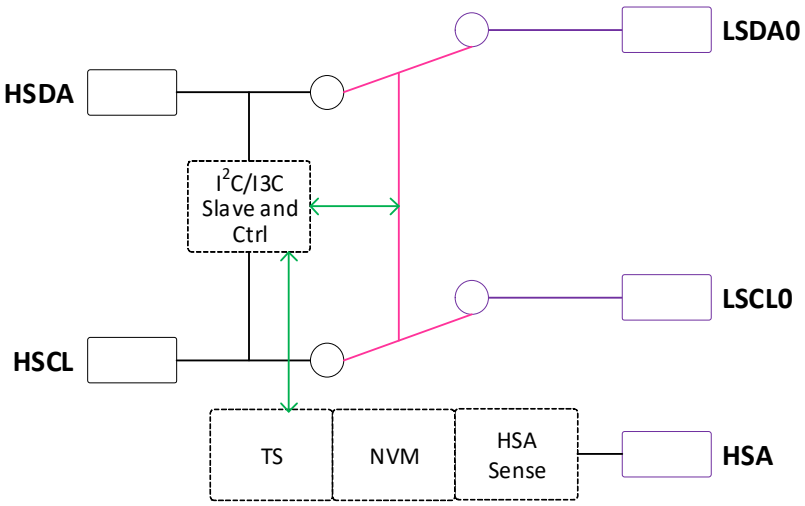


Figure 3. SPD5 Hub Device

2.3 Device Power Up

The SPD5 device has one VDDSPD supply input and one optional VIO supply input.

In order to prevent inadvertent operations during power up, a Power On Reset (POR) circuit is included. On cold power on, VDDSPD input supply must rise monotonically between VPON and $VDDSPD_{min}$ without ringback to ensure proper startup.

The SPD5 device uses the VDDSPD input supply to generate 1.0V LDO output for its IO levels. At power on, the SPD5 device requires the VDDSPD supply input reach power on threshold voltage (V_{PON}) for the SPD5 device to turn on.

2.3.1 SPD5 Hub Device

Once the VDDSPD supply is valid and stable, the SPD5 Hub device shall:

1. Within $t_{1.0V\_Ready}$ time, sense its VIO pin to determine if the SPD5 device has 1.0V input supply present. If not present, enable internal 1.0 V LDO and drive out its internally generated 1.0V LDO output on VIO pin and for its own IO interface.
2. Within t_{Sense_HSA} time, sense its HSA pin to determine if SPD5 Hub device is in application environment or in an offline tester program mode. Depending on what it sense on HSA pin, the SPD5 Hub device configures its HID code automatically based on what it detects on HSA pin at power up. At this point, the SPD5 Hub device may optionally disable the HSA pin and associated sensing circuit.
3. Enable I^2C interface within t_{INIT} time and be ready to receive the command from the host. The SPD5 Hub device is ready for operation after t_{INIT} time.

The host interface HSDA and HSCL signal pins are pulled up to a pull-up voltage through a pull-up resistor on the platform or on the host controller. The pull-up voltage can be available before or after VDDSPD or VDDIO is valid and stable. If HSDA and HSCL pull-up voltage is available before VDDSPD or VDDIO is available, the HSDA and HSCL signal is high and remains high with no leakage path or damage to the SPD Hub device.

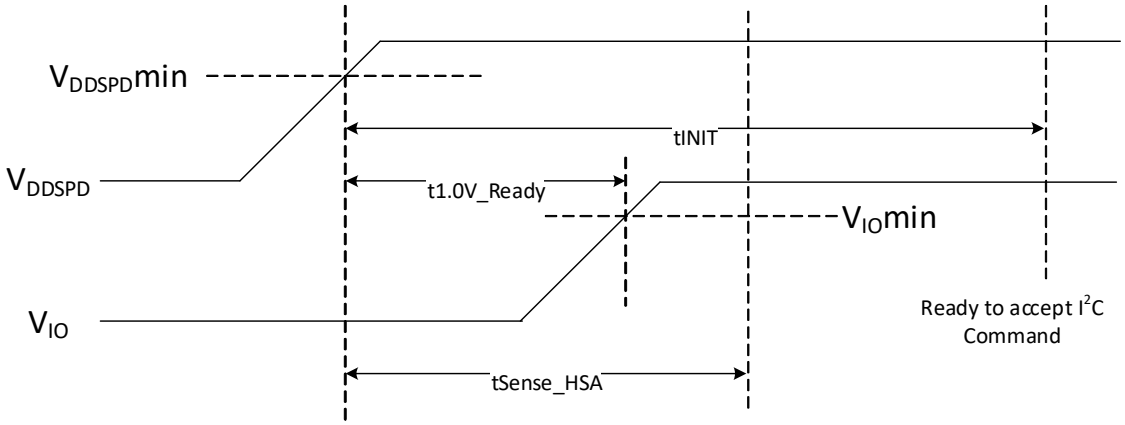


Figure 4. Device Power Up Sequence

2.3.2 DDR5 DIMM Power Up and Bus Readiness

Figure 5 and Figure 6 provide the holistic view of DDR5 RDIMM/LRDIMM power up as reference.

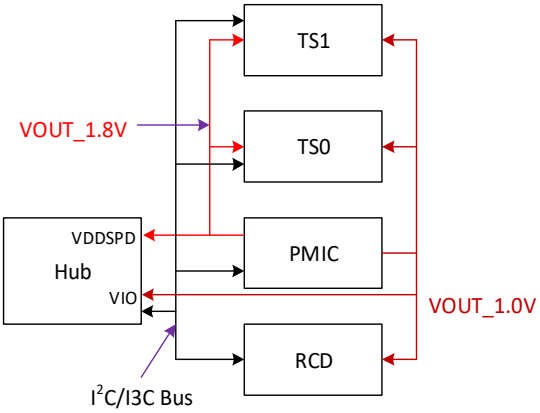
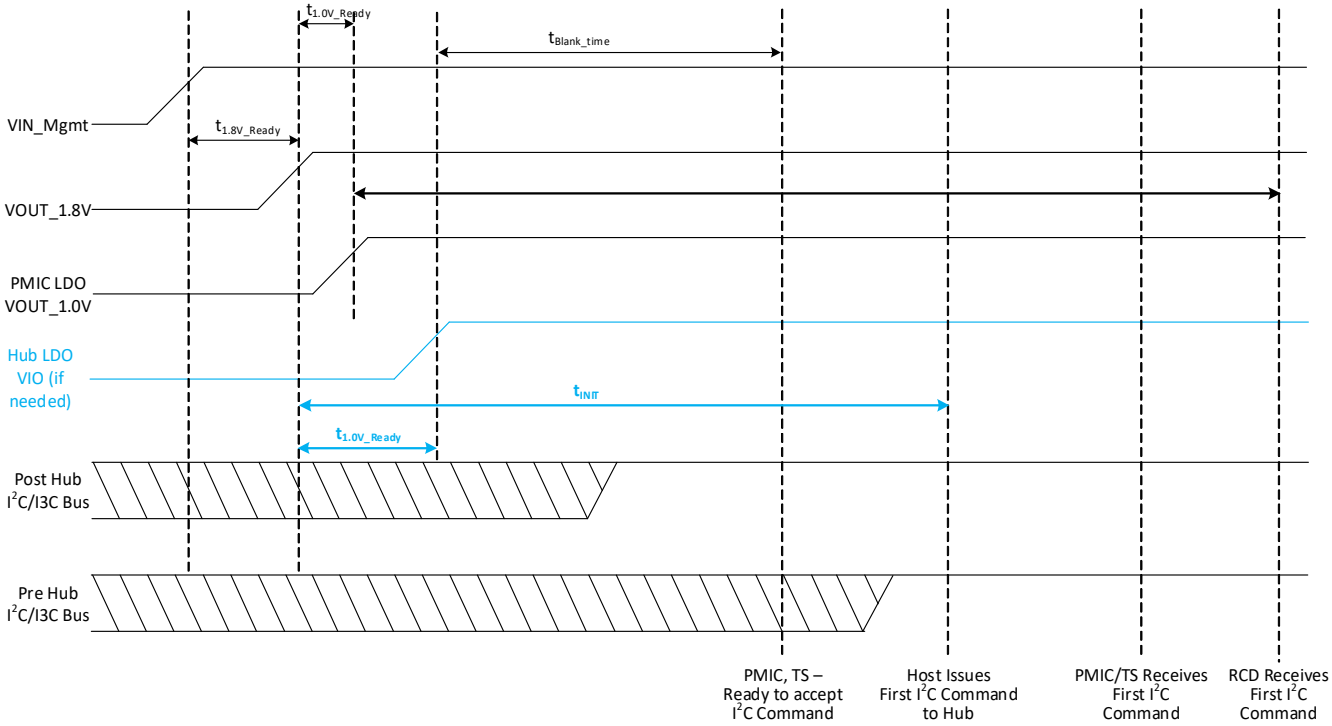


Figure 5. DIMM Power and Bus Topology



PMIC Timing Parameters:
$t_{1.8V\_Ready}$ = 2.5ms Max
$t_{1.0V\_Ready}$ = 1.0ms Max
t_{Blank_time} = 2.0ms Max (i.e Host waits minimum of 2ms)
tManagement_Ready =
x + t_{Blank_time}
Where x = 2ms to 4ms (time for Hub LDO to ramp to valid levels)

Hub Output Timing Parameters:
$t_{1.0V\_Ready}$ = 2.0ms Min; 4.0ms Max

Hub Input Timing Parameters:
t_{INIT} = 10.0ms Min

TS Input Timing Parameters:
$t_{1.8V\_Ready}$ = 2.5ms Max
$t_{1.0V\_Ready}$ = 1.0ms Max
t_{Blank_time} = 2.0ms Max (i.e Host waits minimum of 2ms)

RCD Input Timing Parameters:
$t_{1.0V\_Ready}$ = 1.0ms Max
t_{Blank_time} = 2.0ms Max (i.e Host waits minimum of 2ms)

Figure 6. DIMM Power Sequence and Bus Interface Activity

2.4 Device Reset and Initialization

At power down (phase during which VDDSPD input supply decreases continuously), as soon as VDDSPD input supply drops below the $VDDSPD_{min}$, the device does not guarantee the operation.

On warm power cycling, the VDDSPD and VIO input supply must remain below V_{POFF} for t_{POFF} and must meet cold power on reset timing when restoring the power.

2.5 I^2C and I3C Operation

At power on, by default, the SPD5 Hub device comes up in I^2C mode of operation. Following applies in I^2C mode:

1. The maximum operation speed is limited to 1MHz
2. In-band interrupts are not supported
3. Bus reset is supported.
4. Parity check is not supported except for supported CCCs.
5. Packet Error check is not supported.

The SPD5 devices shall operate in the I^2C mode until placed into I3C Basic mode via command. The host may put the SPD5 Hub device in I3C Basic mode by issuing SETAASA CCC.

The following applies in I3C Basic mode:

1. The maximum operation speed is up to 12.5MHz
2. In-band interrupts are supported
3. Bus reset is supported.
4. Parity check is always enabled by default.
5. Packet error check is supported and by default is disabled.

2.6 Device Interface - IO Voltage Configuration

The SPD5 Hub device supports configurable Open Drain and Push Pull IO levels to accommodate broad range of DDR5 platform and applications.

2.6.1 Open Drain Interface with Internal On Die Pull-up Resistor

The configuration options shown in Figure 7 and Figure 8 are supported when device is in I^2C mode or in I3C Basic mode.

Figure 7 shows the SPD5 Hub device configuration options for Open Drain interface for both Host side and local side of the device. In this configuration, the SPD5 Hub device supports Open Drain IO levels on both Host and Local side. However, the IO voltage levels on Host side and Local side are independent and can be different.

On Host side, the SPD5 device can support IO levels from 1.0 V to 3.3 V depending on the supply rail Host may have pulled up the resistor to. The host side pull-up resistor can be on motherboard or on die inside the host logic device.

On local side, the SPD5 device can support IO levels from 1.0 V to 1.2V and is configurable through MR14[4:2]. For DDR5 DIMM application, DIMM vendor typically sets this register based on the DIMM design and the component selected on the local side of the interface. DIMM vendor also sets the MR14[5] = 0. If the VIO is applied externally, the level should be the same as the setting. If VIO is not applied on the board, the internal LDO of the SPD5 Hub device regulates the VIO output based on the setting of MR14[4:2]. The pull-up resistor selection is configurable and DIMM vendor also sets the register MR15 appropriately.

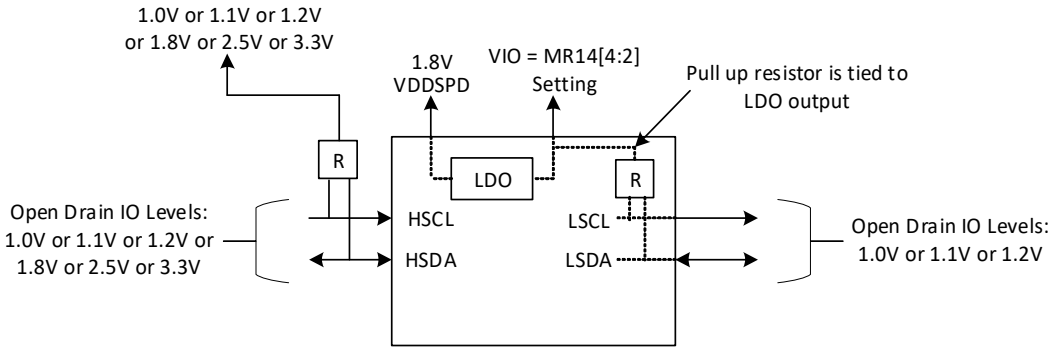


Figure 7. Open Drain Interface; On Die Pull-up to LDO Output

Some application or some components on DIMM may require to support 1.8V IO levels on the local side. Figure 8 shows how SPD5 Hub device supports this configuration. In this configuration, the SPD5 Hub device still supports Open Drain IO levels on both Host and Local side. However, the IO voltage levels on Host side and Local side are independent and can be different.

MR14[4:2] should be set to the local side pull-up IO level. If the local side IO pull-up voltage is 1.8V, set the MR[4:2] = 011, the SPD5108/SPD5118 internally connects VDDSPD to VIO via a switch. In this case, it is suggested to connect the VIO to VDDSPD directly on the board. MR14[5] disables the internal pull-up. The internal pull-up connects to the VIO rail, and only works if the local side IO voltage setting is 000, 001, 010, or 011. The pull-up resistor selection is configurable and DIMM vendor also sets the register MR15 appropriately.

The host side can still support any IO levels from 1.0V to 3.3V depending on the supply rail Host may have pulled up the resistor to.

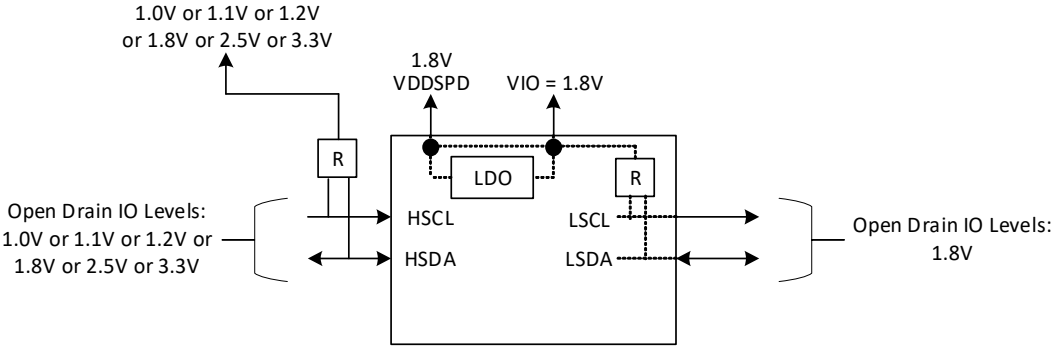


Figure 8. Open Drain Interface; MR14[4:2] = 011

2.6.2 Open Drain Interface with External Pull-up Resistor

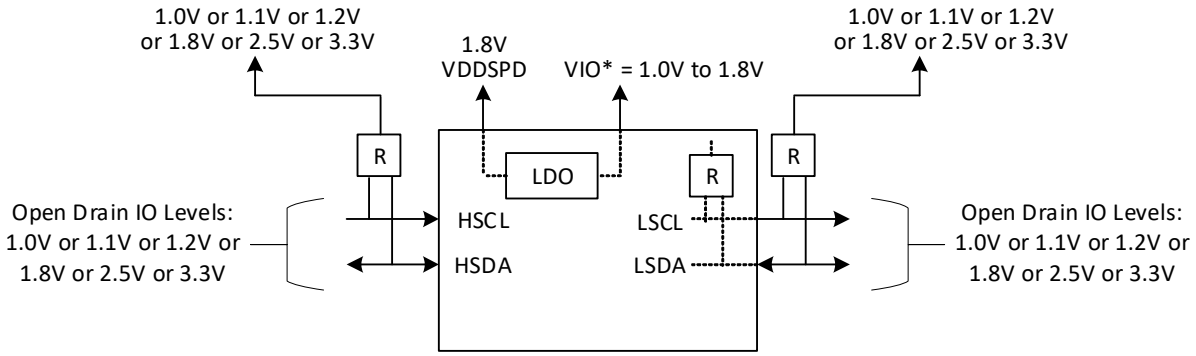
The configuration options shown in Figure 9 is supported when device is in I^2C mode or in I3C Basic mode.

Figure 9 shows the SPD5 Hub device configuration options for Open Drain interface for both Host side and local side of the device. In this configuration, the SPD5 device supports Open Drain IO levels on both Host and Local side. However, the IO voltage levels on Host side and Local side are independent and can be different.

On Host side, the SPD5 Hub device can support IO levels from 1.0V to 3.3V depending on the supply rail Host may have pulled up the resistor to. The host side pull-up resistor can be on motherboard or on die inside the host logic device.

On local side, the SPD5 device can support IO levels from 1.0V to 3.3V and is configurable through MR14 [4:2]. MR14 [4:2] should set to the level of the local side external pull-up voltage. If the VIO is applied externally, the level should be the same as the setting, and saturate to 1.8V. If the IO pull-up voltage is greater than 1.8V, VIO should be set to 1.8V. If VIO is not applied, it will be set to 1.8V internally.

For DDR5 DIMM application, DIMM vendor typically sets this register based on the DIMM design (i.e. how the supply rail of the external pull-up resistor). DIMM vendor also sets the MR14 [5] = 1. The setting of the register MR15 [7:0] is not applicable. The internal LDO of the SPD5 device regulation is design specific.



* If local OD IO voltage is higher than 1.8V, VIO just needs to set to 1.8V.

Figure 9. Open Drain Interface; External On Board Pull-up Resistor

2.6.3 Push Pull Interface with Internal On Die Pull-up Resistor

The configuration option shown in Figure 10 is only supported when device is in I3C Basic mode.

Figure 10 shows the SPD5 Hub device configuration options for Push Pull interface for both Host side and local side of the device. In this configuration, the SPD5 Hub device supports Push Pull IO levels on both Host and Local side. However, the IO voltage levels on Host side and Local side are independent and can be different.

On Host side, the SPD5 Hub device can support IO levels from 1.0V to 1.2V or 1.8V. The host side pull-up resistor can be on motherboard or on die inside the host logic device.

On local side, the SPD5 Hub device can support IO levels from 1.0V to 1.2V or 1.8V and is configurable through MR14 [4:2]. For DDR5 DIMM application, DIMM vendor typically sets this register based on the DIMM design and the component selected on the local side of the interface. DIMM vendor must sets the MR14 [5] = 0. If VIO is applied externally on the board, it should be applied at the same level as configured in MR14[4:2]. If VIO is not applied on the board, the internal LDO of the SPD5 Hub device regulates its output based on the setting of the MR14 [4:2]. The pull-up resistor selection is configurable and DIMM vendor also sets the register MR15 appropriately.

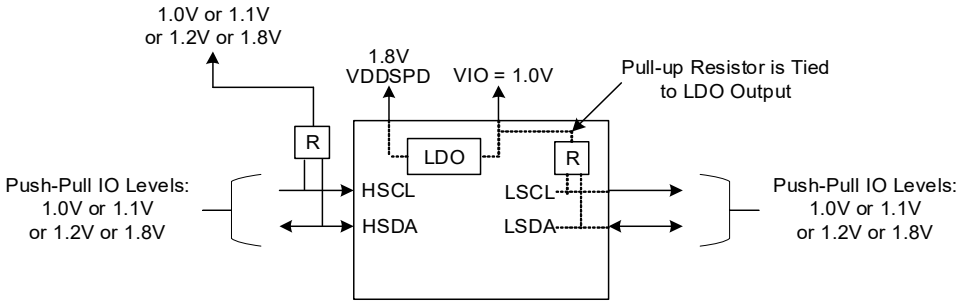


Figure 10. Push Pull Interface; On Die Pull-up to LDO Output

2.7 Management Bus Protocol

The 7-bit serial address of the SPD5 Hub device and all local devices behind the Hub applies to both I^2C and I3C Basic mode of operation identically.

2.7.1 Serial Address of the SPD5 Hub Device

The SPD5 Hub device type ID is 4-bit binary value of 1010b.

The SPD5 Hub device samples the status of the HSA pin on power up. The status of the HSA pin determine the unique host ID (HID) of the device. The host identifier value is merged with the SPD5 Hub device type 1010 xxxb to establish the 7-bit address (SPD5 Hub select code) for this device on the I^2C or I3C Basic bus as shown in Table 4. For example, if the value sensed on HSA pin identifier 2 (010 binary), then the unique address for this device is 1010 010b.

Table 4. 7-Bit Address of the SPD5 Hub Device

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	0	HID2	HID1	HID0	R/W
SPD5 Hub Device Type ID				Host ID (HID)			Read/Write

2.7.2 Serial Address of the Local Devices

Each local device behind the SPD5 Hub device has a unique 4 bit local device ID (LID) code. For example the PMIC local device type ID is 4-bit binary value of 1001b.

The 3 HID bits of the local device type has a default value of 111 and is merged with its unique 4 bit local ID code to establish the 7-bit address for the local device on the I^2C or I3C Basic bus as shown in Table 5. For example, the PMIC local device behind the SPD Hub has 7-bit address of 1001 111b.

Table 5. 7-Bit Address of the Local Devices (e.g. PMIC Device)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	1	1	1	1	R/W
Local Device Type ID (LID)				Host ID (HID)			Read/Write

2.7.3 Switch from I^2C Mode to I3C Basic Mode

By default when SPD5 Hub first powers on, it operates in I^2C mode. The SPD5 Hub device shall operate in I^2C mode until put into I3C Basic mode via command.

In I^2C mode, the host is allowed to issued only 3 CCCs (DEVCTRL, SETHID, SETAASA). All other CCCs are not supported and considered an illegal operation and the SPD5 Hub device may simply ignore it. The Host must issue DEVCTRL and SETHID CCC first (if required) followed by SETAASA CCC.

When SETHID CCC is registered by the SPD5 Hub device, it stops the 3-bit HID translation for the local slave device as explained in Local Device Selection Through the SPD5 Hub Device (Before SETHID CCC).

The Host puts the SPD5 Hub device in I3C mode by issuing SETAASA CCC.

When SETAASA CCC is registered by the SPD5 Hub device, it updates the MR18 [5] and INF_SEL bit in GETSTATUS CCC to 1.

2.7.4 Switch from I3C Basic Mode to I^2C Mode

The Host can put the SPD5 Hub back in I^2C mode from I3C Basic mode at any time by issuing RSTDAA CCC.

When RSTDAA CCC is registered by the SPD5 Hub device, it updates the MR18 [5] and INF_SEL bit in GETSTATUS CCC to 0.

2.7.5 SPD5 Hub Device Selection

The host can access any SPD5 Hub device as shown in Table 6 in both I^2C mode and I3C Basic mode. The last 3 bits represent the HID bits.

Table 6. 7-Bit Address of Each Hub Devices on I²C/I3C Basic Bus

Host Access to:	7-Bit Address
DIMM 0 SPD Hub	1010 000
DIMM 1 SPD Hub	1010 001
DIMM 2 SPD Hub	1010 010
DIMM 3 SPD Hub	1010 011
DIMM 4 SPD Hub	1010 100
DIMM 5 SPD Hub	1010 101
DIMM 6 SPD Hub	1010 110
DIMM 7 SPD Hub	1010 111

2.7.6 Local Device Selection Through the SPD5 Hub Device (Before SETHID CCC)

By default, the SPD5 Hub device and all local slave devices powers up in I²C mode of operation, Prior to Host issuing SETHID CCC, the host can access the any local device behind the SPD5 Hub device. To access the local device, the host sends 7-bit address that is made up of 4 bits of local device code (LID) followed by the 3 bits of HID code. The LID code represents which local device host is intended to target. The HID code represents which DIMM the local device resides on. The Table 7 shows an example of four different local device address codes behind SPD5 Hub on each DIMM.

Table 7. 7-Bit Address of Local Devices on I²C/I3C Basic Bus

Host Access to:	7-bit Address LID = 1011 (RCD)	7-bit Address LID = 1001 (PMIC)	7-bit Address LID = 0010 (TS0)	7-bit Address LID = 0110 (TS1)
DIMM 0 Local Device	1011 000	1001 000	0010 000	0110 000
DIMM 1 Local Device	1011 001	1001 001	0010 001	0110 001
DIMM 2 Local Device	1011010	1001 010	0010 010	0110 010
DIMM 3 Local Device	1011 011	1001 011	0010 011	0110 011
DIMM 4 Local Device	1011 100	1001 100	0010 100	0110 100
DIMM 5 Local Device	1011 101	1001 101	0010 101	0110 101
DIMM 6 Local Device	1011 110	1001 110	0010 110	0110 110
DIMM 7 Local Device	1011 111	1001 111	0010 111	0110 111

The SPD5 Hub Device monitors the LID code coming from the host. When it detects the host access is for the slave device, it compares the last 3 bits of the HID information (shown in Red) coming from the host against its own unique HID code that it has stored at power on. It compares each 3 bits one at a time. If there is a match, the SPD5 Hub device substitutes that bit with 1 and forward it to the local device interface. If there is a mis-match, the SPD5 Hub device substitutes that bit with 0 and forwards it to the local device interface. As a result, only the targeted local device will see its last three HID bits as 111 and all non-targeted local devices will see its last three HID bits as anything other than 111 which is not a valid code as shown in Table 5.

There are two exceptions when SPD5 Hub device does not substitute its own HID code when it forwards it to the local slave interface:

1. Host issues Start followed by 7'h7E with W = 0 (or Host issues Start followed by 0xFC).
2. After SPD5 Hub executes SETHID CCC command that Host issues. See Local Device Selection Through the SPD5 Hub Device (After SETHID CCC).

Figure 11 gives an example of Host accessing local RCD Device on DIMM0. The figure shows Host sends 7-bit address 1011 000. Each SPD5 Hub devices receives this address. Each SPD5 Hub device forward first four bits

of binary address 1011 (LID) on the local device interface. Each SPD5 Hub compares last 3 bits of binary address 000 from the host against its own unique HID code and substitutes the bit on the local device interface.

	Hub SPD		RCD		PMIC0		PMIC1		PMIC2		TS0		TS1	
DIMM0	101 0000	50	**101 1111**	**5F**	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F
DIMM1	101 0001	51	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E
DIMM2	101 0010	52	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D
DIMM3	101 0011	53	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C
DIMM4	101 0100	54	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B
DIMM5	101 0101	55	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A
DIMM6	101 0110	56	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59
DIMM7	101 0111	57	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58

Figure 11. Example: Host Accessing RCD on DIMM 0

Figure 12 gives another example of Host accessing local Temperature Sensor 0 device on DIMM3. The figure shows Host sends 7-bit address 0010 011. Each SPD5 hub devices receives this address. Each SDP5 Hub device forward first four bits of binary address 0010 (LID) on the local device interface. Each SPD5 Hub compares last 3 bits of binary address 011 from the host against its own unique HID code and substitutes the bit on the local device interface.

	Hub SPD		RCD		PMIC0		PMIC1		PMIC2		TS0		TS1	
DIMM0	101 0000	50	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0100	14	001 0100	14	001 0100	14	001 0100	14	001 0100	14	001 0100	14
DIMM1	101 0001	51	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0101	15	001 0101	15	001 0101	15	001 0101	15	001 0101	15	001 0101	15
DIMM2	101 0010	52	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0110	16	001 0110	16	001 0110	16	001 0110	16	001 0110	16	001 0110	16
DIMM3	101 0011	53	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	**001 0111**	**17**	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0111	17	001 0111	17	001 0111	17	001 0111	17	001 0111	17	001 0111	17
DIMM4	101 0100	54	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0000	10	001 0000	10	001 0000	10	001 0000	10	001 0000	10	001 0000	10
DIMM5	101 0101	55	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0001	11	001 0001	11	001 0001	11	001 0001	11	001 0001	11	001 0001	11
DIMM6	101 0110	56	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0010	12	001 0010	12	001 0010	12	001 0010	12	001 0010	12	001 0010	12
DIMM7	101 0111	57	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0011	13	001 0011	13	001 0011	13	001 0011	13	001 0011	13	001 0011	13

Figure 12. Example: Host Accessing Temperature Sensor 0 on DIMM 3

2.7.7 Local Device Selection Through the SPD5 Hub Device (After SETHID CCC)

When SETHID CCC is registered by the SPD5 Hub device, it stops the 3-bit HID translation for the local slave device as explained in Local Device Selection Through the SPD5 Hub Device (Before SETHID CCC). After Host sends SETHID CCC, the Host still accesses all the slave devices behind the SPD5 Hub as shown in Table 7. There is no change in how Host access the SPD5 Hub device and all local slave devices behind the SPD5 Hub device before or after SETHID CCC.

2.7.8 I²C Slave Protocol - Host to SPD5 Hub Device

The SPD5 Hub devices operate on a standard I²C serial interface. Transactions where the SPD5 Hub device is the targeted slave device begin with the Host issuing a START condition followed by a 7-bit SPD5 Hub device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the SPD5 Hub device typically replies with an ACK unless there are conditions when it may passively assert a NACK.

The SPD5 Hub device does not allow any read or write operation to its non-volatile memory when it is busy with internal write operation to non-volatile memory. The host should either check MR48 [3] register status or ensure that Write time (t_W) parameter is satisfied prior to performing another write or read to operation to non-volatile memory. If host violates this and performs either write or read operation to non-volatile memory then SPD5 Hub device ACKs the device address byte to allow possible volatile register access. However, the SPD5 Hub device NACKs the subsequent write or read operation if MemReg = 1 and sets the MR52 [7] = 1.

The SPD5 Hub device does allow any read or write operation to its volatile memory (i.e. MemReg = 0) when it is busy with internal write operation to non-volatile memory.

To allow compatibility with legacy I2C host controller, the SPD5 Hub device offers two ways to address 1024 bytes of non-volatile memory when it is operating in I2C mode only. By default, the SPD5 Hub device accepts 1 byte of address which covers first 128 bytes of non-volatile memory. The host must select the page pointer through volatile register MR11 [2:0] to address the entire 1024 bytes of non-volatile memory.

Alternatively, at initial power on, the host can set the MR11 [3] = 1 to address the entire 1024 bytes of non-volatile memory with 2 bytes of address and hence not required to go through page selection to address entire non-volatile memory.

This 1 byte address mode is only applicable to SPD5 Hub device and it is not applicable to PMIC or TS or RCD device in I2C mode.

The SPD5 Hub device volatile register space does not require the page selection process as all volatile registers are within first 128 bytes.

2.7.8.1 Write Operation - Data Packet

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = 1) or an internal register (MemReg = 0). When MemReg = 0, there is no concept of “Block Address”; Block Address bits are treated simply Upper Address bits.

Table 8. Write Command Data Packet; MR11 [3] = 0

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	1	0	HID			W = 0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	Data								A	
	...								A	
	Data								A	Sr or P (Note 2)

1. In I2C mode, Start or Repeat Start operation followed by 7’h7E with W = 0 is only allowed for CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. All write transactions to NVM location (MemReg = 1) shall terminate with STOP operation (i.e. no Repeat Start is allowed for NVM operation).

Table 9. Write Command Data Packet; MR11 [3] = 1

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	1	0	HID			W = 0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	0	0	0	0	Blk Addr [4:1] (Note 2)				A	
	Data								A	
	...								A	
	Data								A	Sr or P (Note 3)

1. In I2C mode, Start or Repeat Start operation followed by 7’h7E with W = 0 is only allowed for CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. The memory size of SPD hub device is limited to 1024 Bytes. SPD Hub device ignores Blk Addr [4] bit.
3. All write transactions to NVM location (MemReg = 1) shall terminate with STOP operation (i.e. no Repeat Start is allowed for NVM operation).

2.7.8.2 Read Operation - Data Packet

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = 1) or an internal register (MemReg = 0). When MemReg = 0, there is no concept of “Block Address”; Block Address bits are treated simply Upper Address bits.

Table 10. Read Command Data Packet; MR11 [3] = 0

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	1	0	HID			W = 0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
Sr	1	0	1	0	HID			R = 1	A (Note 2)	
	Data								A	
	...								A	
	Data								N	Sr or P

1. In I2C mode, Start or Repeat Start operation followed by 7’h7E with W = 0 is only allowed for CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required.

Table 11. Read Command Data Packet; MR11 [3] = 1

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	1	0	HID			W = 0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	0	0	0	0	Blk Addr [4:1] (Note 2)				A	
Sr	1	0	1	0	HID			R = 1	A (Note 3)	
	Data								A	
	...								A	
	Data								N	Sr or P

1. In I2C mode, Start or Repeat Start operation followed by 7’h7E with W = 0 is only allowed for CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. The memory size of SPD hub device is limited to 1024 Bytes. SPD Hub device ignores Blk Addr [4] bit.
3. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required.

2.7.8.3 Default Read Address Pointer Mode

During normal operation of the DDR5 DIMM, the host periodically may poll critical information from the same location. An example may be the SPD5 Hub device’s temperature readout. To help improve the efficiency of the I2C bus protocol, the SPD5 Hub offers a default read address pointer mode so that whenever the SPD5 Hub device sees the STOP operation on its HSCL and HSDA bus, its read address pointer is always resets to default address. The default read pointer address mode is enabled through register MR18 [4] and default starting address for read operation is selectable through register MR18 [3:2]. This allows host to read the read command data packet as shown in Table 12 from Table 11. The default read address pointer reduces the packet overhead by 3 bytes. The host typically enables this mode when the normal operation of the DDR5 DIMM begins. The default read address pointer mode is only applicable to volatile register space (i.e. MemReg = 0).

Table 12. Read Command Data Packet with Default Address Pointer Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	1	0	1	0	HID			R = 1	A	
	Data								A	
	...								A	
	Data								N	Sr or P

The Default Read Address Pointer mode can be used in conjunction with other normal Write and Read operation. There is only one address pointer. If Default Read Address Pointer mode is enabled, the address pointer always resets to the address selected by MR18 [3:2] when device sees STOP operation. When there is no STOP operation, the address pointer always advances to next address for any write or read transactions or for write followed by read and read followed by write transactions.

Table 13 gives an example of write followed by read transaction with Repeat Start operation. For write transaction, the host performs the write operation to address 0x15 and provides 3 bytes of data. The device increments the address counter to 0x18 when 3 bytes of data is written. When host does the read transaction with Repeat Start, the device returns the data from where the previous address pointer was left which is at address 0x18.

Table 13. Write Command followed by Read Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	0	HID			W = 0	A	
	Address [7:0] (i.e. 0x15)								A	
	Data (at address 0x15)								A	
	Data (at address 0x16)								A	
	Data (at address 0x17)								A	
Sr	1	0	1	0	HID			R = 1	A	
	Data (from address 0x18)								A	
	Data (from address 0x19)								N	P

Table 14 gives an example of write followed by Stop operation followed by a read transaction with Start operation. For write transaction, the host performs the write operation to address 0x15 and provides 3 bytes of data. The host then performs Stop operation and does Start operation. The device resets the address pointer because of STOP operation as default read address pointer mode is enabled, it returns the data from address 0x08.

Table 14. Write Command followed by Read Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	0	HID			W = 0	A	
	Address [7:0] (i.e. 0x15)								A	
	Data (at address 0x15)								A	
	Data (at address 0x16)								A	
	Data (at address 0x17)								A	P
S	1	0	1	0	HID			R = 1	A	
	Data (from address 0x08)								A	
	Data (from address 0x09)								N	P

Table 15 gives an example of read followed by read transaction with Repeat Start operation. For read transaction, the host provides the address 0x15 for device to return the data. The device returns the data from address 0x15 and 0x16. When host does the read transaction with Repeat Start, the device returns the data from where the previous address pointer was left which is at address 0x17.

Table 15. Read Command followed by Read Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	0	HID			W = 0	A	
	Address [7:0] (i.e. 0x15)								A	
Sr	1	0	1	0	HID			R = 1	A	
	Data (from address 0x15)								A	
	Data (from address 0x16)								N	
Sr	1	0	1	0	HID			R = 1	A	
	Data (from address 0x17)								A	
	Data (from address 0x18)								N	P

Table 16 gives an example of read followed by default read pointer mode read transaction. For read transaction, the host provides the address 0x15 for device to return the data. The device returns the data from address 0x15 and 0x16. The host then perform the STOP operation and does Start operation. The device resets the address pointer because of STOP operation as default read address pointer mode is enabled, it returns the data from address 0x08.

Table 16. Read Command followed by Default Read Pointer Mode Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	0	HID			W = 0	A	
	Address [7:0] (i.e. 0x15)								A	
Sr	1	0	1	0	HID			R = 1	A	
	Data (from address 0x15)								A	
	Data (from address 0x16)								N	P
S	1	0	1	0	HID			R = 1	A	
	Data (from address 0x08)								A	
	Data (from address 0x09)								N	P

Table 17 gives an example of default read pointer mode followed repeat start operation followed read operation. For default read operation mode read transaction, the device returns the data from address 0x08, 0x09 and the address pointer is at 0x0A. The host then performs Repeat Start operation followed by Read operation. Because the device does not see the Stop operation, the address pointer does not get reset and the device returns the data from the address 0x0A, 0x0B.

Table 17. Read Command followed by Read Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	0	HID			R = 1	A	
	Data (from address 0x08)								A	
	Data (from address 0x09)								N	
Sr	1	0	1	0	HID			R = 1	A	
	Data (from address 0x0A)								A	
	Data (from address 0x0B)								N	P

Table 18 gives an example of consecutive default read address pointer mode transactions to four different devices (PMIC, TS0, TS1, and SPD Hub). This example assumes that host has performed STOP operation previously. The host performs Start operation followed by default read address pointer mode operation to four different devices, PMIC, TS0, TS1, SPD Hub consecutively, in order, with Repeat Start operation. The PMIC returns the data from address 0x08, 0x09, 0x0A, 0x0B; the TS0 returns the data from address 0x31, 0x32; the TS1 returns the data from address 0x31, 0x32; the SPD Hub returns the data from address 0x31, 0x32, 0x33, 0x34. The host then performs Stop operation.

Table 18. Consecutive Default Read Pointer Mode Command Data Packets

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	0	1	HID			R = 1	A	
	Data (from address 0x08)								A	
	Data (from address 0x09)								A	
	Data (from address 0x0A)								A	
	Data (from address 0x0B)								N	
Sr	0	1	1	0	HID			R = 1	A	
	Data (from address 0x31)								A	
	Data (from address 0x32)								N	
Sr	0	0	1	0	HID			R = 1	A	
	Data (from address 0x31)								A	
	Data (from address 0x32)								N	
Sr	1	0	1	0	HID			R = 1	A	
	Data (from address 0x31)								A	
	Data (from address 0x32)								A	
	Data (from address 0x33)								A	
	Data (from address 0x34)								N	P

2.7.9 I²C Slave Protocol - Host to Local Device Through SPD5 Hub Device

2.7.9.1 Write Operation - Data Packet

Table 19. Write Command Data Packet (e.g. TS0)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	0	0	1	0	HID			W = 0	A	
	Address [7:0]								A	
	Data								A	
	Data								A	
	...								A	
	Data								A	Sr or P

1. In I²C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation.

Table 20. Write Command Data Packet (e.g. PMIC)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	0	1	HID			W = 0	A	
	Address [7:0]								A	
	Data								A	
	Data								A	
	...								A	
	Data								A	Sr or P

1. In I2C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.

When Host makes any write request to the RCD device, the RCD protocol has PEC check in the last byte. The SPD simply treats the last byte as Data like any other bytes as shown in Table 22. The RCD device requires valid stable input clock (DCK_t, DCK_c), Reset_n and DCS_n to allow any read or write access on its I2C interface.

Table 21. Write Command Data Packet (e.g. RCD; PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	1	1	HID			W = 0	A	
	Data (I2C Bus Command)								A	
	Data (Byte Count=8)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	
	Data (Wr Data [31:24])								A	
	Data (Wr Data [23:16])								A	
	Data (Wr Data [15:8])								A	
	Data (Wr Data [7:0])								A	Sr or P

1. In I2C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.

Table 22. Write Command Data Packet (e.g. RCD; PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	1	1	HID			W = 0	A	
	Data (I^2C Bus Command)								A	
	Data (Byte Count=8)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	
	Data (Wr Data [31:24])								A	
	Data (Wr Data [23:16])								A	
	Data (Wr Data [15:8])								A	
	Data (Wr Data [7:0])								A	
	Data (PEC [7:0])								A	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.

2.7.9.2 Read Operation - Data Packet

Table 23. Read Command Data Packet (e.g. TS0)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	0	0	1	0	HID			W = 0	A	
	Address [7:0]								A	
Sr	0	0	1	0	HID			R = 1	A (Note 2)	
	Data								A	
	Data								A	
	...								A	
	Data								N	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required.

Table 24. Read Command Data Packet (e.g. PMIC)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	0	1	HID			W = 0	A	
	Address [7:0]								A	
Sr	1	0	0	1	HID			R = 1	A (Note 2)	
	Data								A	
	Data								A	
	...								A	
	Data								N	Sr or P

1. In I2C mode, Start or Repeat Start operation followed by 7'7h7E with W = 0 is only allowed for CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If slave device NACKs during Repeat Start for any reason, the host my retry Repeat Start again. The host can do the Repeat Start as many times as required.

When Host makes any read request to the RCD device, the RCD protocol has PEC check for the RCD address information as well as data returned by the RCD. The SPD simply treats the PEC information as simply data byte like any other data. The SPD Hub device does not check for the PEC.

Table 25. Read Command Data Packet (e.g. RCD; PEC Disabled; Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	1	1	HID			W = 0	A	
	Data (I2C Bus Command)								A	
	Data (Byte Count = 4)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	Sr or P
S or Sr	1	0	1	1	HID			W = 0	A	
	Data (I2C Bus Command)								A	
Sr	1	0	1	1	HID			R = 1	A (Note 2)	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data [31:24])								A	
	Data (Rd Data [23:16])								A	
	Data (Rd Data [15:8])								A	
	Data (Rd Data [7:0])								N	Sr or P

1. In I2C mode, Start or Repeat Start operation followed by 7'7h7E with W = 0 is only allowed for CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required.

Table 26. Read Command Data Packet (e.g. RCD; PEC Enabled; Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	1	1	HID			W = 0	A	
	Data (I^2C Bus Command)								A	
	Data (Byte Count = 4)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	
	Data (PEC [7:0])								A	Sr or P
S or Sr	1	0	1	1	HID			W = 0	A	
	Data (I^2C Bus Command)								A	
Sr	1	0	1	1	HID			R = 1	A (Note 2)	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data [31:24])								A	
	Data (Rd Data [23:16])								A	
	Data (Rd Data [15:8])								A	
	Data (Rd Data [7:0])								A	
	Data (PEC [7:0])								N	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'7h7E with W = 0 is only allowed for CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required.

Table 27. Read Command Data Packet (e.g. RCD; PEC Disabled; Optimized Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr (Note 1)	1	0	1	1	HID			W = 0	A	
	Data (I^2C Bus Command)								A	
	Data (Byte Count = 4)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	
Sr	1	0	1	1	HID			R = 1	A (Note 2)	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data [31:24])								A	
	Data (Rd Data [23:16])								A	
	Data (Rd Data [15:8])								A	
	Data (Rd Data [7:0])								N	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'7h7E with W = 0 is only allowed for CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required.

2.7.10 I3C Basic Slave Protocol - Host to SPD5 Hub Device

2.7.10.1 Write Operation Data Packet

The SPD5 Hub devices operate on a standard I3C Basic serial interface. Transactions where the SPD5 Hub device is the targeted slave device begin with the Host issuing a START condition followed by a 7-bit SPD5 Hub device address then a write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the SPD5 Hub device typically replies with an ACK unless there are conditions when it may passively assert a NACK. The T bit carries Parity information from the Host for each byte.

The SPD5 Hub device does not allow any read or write operation to its non-volatile memory when it is busy with internal write operation to non-volatile memory. The host should either check MR48 [3] register status or ensure that Write time (t_w) parameter is satisfied prior to performing another write or read to operation to non-volatile memory. If host violates this and performs either write or read operation to non-volatile memory then SPD5 Hub device always ACKs the device address byte. In a subsequent byte, the device ignores the write operation if MemReg = 1 and sets the MR52 [7] = 1 and requests IBI if IBI function is enabled. Subsequently, if host continues to do the read operation with Repeat Start, the SPD5 Hub device NACKs.

The SPD5 Hub device does allow any read or write operation to its volatile memory (i.e. MemReg = 0) when it is busy with internal write operation to non-volatile memory.

The Packet Error Code (PEC) function is disabled by default when the SPD5 Hub device is put in I3C Basic mode. The host may optionally enable this function through MR18 [7] or DEVCTRL CCC. If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length prematurely for Write operation.

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = 1) or an internal register (MemReg = 0). When MemReg = 0, there is no concept of “Block Address”; Block Address bits are treated simply Upper Address bits.

Table 28. Write Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] (Note 4)				T	
	Data								T	
	...								T	
	Data								T	Sr (Note 5) or P (Note 6)

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
5. Repeat Start or Repeat Start with 7'h7E.
6. All write transactions to NVM location (MemReg = 1) shall terminate with STOP operation (i.e. no Repeat Start is allowed for NVM operation).

Table 29. Write Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			W = 0	Blk Addr [4:1] (Note 4)				T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr (Note 5) or P (Note 6)

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity error or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
5. Repeat Start or Repeat Start with 7'h7E.
6. All write transactions to NVM location (MemReg = 1) shall terminate with STOP operation (i.e. no Repeat Start is allowed for NVM operation).

The host may optionally allow SPD5 Hub device to request IBI. For this case, the transactions to the SPD5 Hub device begin with the I3C Basic host issuing a START condition followed by 7'h7E and then write bit. If SPD5 Hub device has a pending IBI, it transmits its 7-bit device select code followed by R = 1. If SPD5 Hub device has no pending IBI, there is no action taken by SPD5 Hub. Table 30 and Table 31 show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. **Note:** In Table 31, PEC calculation does not include IBI header byte (7'h7E followed by W = 0).

Table 30. Write Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Notes 1, 3)	
Sr	1	0	1	0	HID			W = 0	A (Notes 2, 3, 4)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] (Note 5)				T	
	Data								T	
	...								T	
	Data								T	Sr (Note 6) or P (Note 7)

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK) and Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
3. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
4. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
5. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
6. Repeat Start or Repeat Start with 7'h7E.
7. All write transactions to NVM location (MemReg = 1) shall terminate with STOP operation (i.e. no Repeat Start is allowed for NVM operation).

Table 31. Write Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Notes 1, 3)	
Sr	1	0	1	0	HID			W = 0	A (Notes 2, 3, 4)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			W = 0	Blk Addr [4:1] (Note 5)				T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr (Note 6) or P (Note 7)

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK) and Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
3. The SPD5 Hub NACKs if there is a parity error or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
4. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
5. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
6. Repeat Start or Repeat Start with 7'h7E.
7. All write transactions to NVM location (MemReg = 1) shall terminate with STOP operation (i.e. no Repeat Start is allowed for NVM operation).

2.7.10.2 Read Operation Data Packet

The transactions to SPD5 Hub slave device begin with the I3C Basic Host issuing a START condition followed by a 7-bit SPD5 Hub device type identifier then a write bit. All I3C Basic bus data are transmitted with the most significant bit MSB first. During select code transmission, the SPD5 Hub device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 32. The T bit carries Parity information from the host prior to Repeated START. After Repeated START, T bit carries information from SPD5 Hub device to Host indicating Continuous (1) or Stop (0) whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when SPD5 Hub device is put in I3C Basic mode. The host may optionally enable this function through MR18 [7] or DEVCTRL CCC. If enabled, the PEC is appended as shown in Table 33. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length prematurely for Read operation

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = 1) or an internal register (MemReg = 0). When MemReg = 0, there is no concept of "Block Address"; Block Address bits are treated simply Upper Address bits.

Table 32. Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] (Note 4)				T	
Sr	1	0	1	0	HID			R = 1	A/N (Notes 5, 6)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1 (Notes 7, 8)	Sr (Note 9) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD hub device is limited to 1024 Bytes. SPD Hub device ignores Blk Addr [4] bit.
5. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the SPD Hub may eventually ACK.
6. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
7. Figure 16 shows how the Host ends slave device operation.
8. For NVM read memory access (i.e. MemReg = 1), when last byte is reached (1024 Byte) or for volatile memory access (i.e. MemReg = 0), when last byte (i.e. MR255) is reached (extreme rare case), the slave device sends T = 0. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
9. Repeat Start or Repeat Start with 7'h7E.

Table 33. Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W = 0	A(Notes 1, 2, 3)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			R = 1	Blk Addr [4:1] (Note 4)				T	
	PEC								T	
Sr	1	0	1	0	HID			R = 1	A/N (Notes 5, 6)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1	
	PEC								T = 0 (Note 7)	Sr (Note 8) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD Hub device is limited to 1024 Bytes. SPD Hub device ignores Blk Addr [4] bit.
5. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the SPD Hub may eventually ACK. The PEC calculation by the slave device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the slave device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
6. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
7. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
8. Repeat Start or Repeat Start with 7’h7E.

The host may optionally allow SPD5 Hub device to request IBI. For this case, the transactions to the SPD5 Hub device begin with the I3C Basic host issuing a START condition followed by 7’h7E and then write bit. If SPD5 Hub device has a pending IBI, it transmits its 7-bit device select code followed by R = 1. If SPD5 Hub device has no pending IBI, there is no action taken by SPD5 Hub. Table 34 and Table 35 show the I3C Basic bus read command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. **Note:** In Table 35, PEC calculation (from Host to SPD5 Hub) does not include IBI header byte (7’h7E followed by W = 0).

Table 34. Read Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Notes 1, 3)	
Sr	1	0	1	0	HID			W = 0	A (Notes 2, 3, 4)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] (Note 5)				T	
Sr	1	0	1	0	HID			R = 1	A/N (Notes 6, 7)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1 (Notes 8, 9)	Sr (Note 10) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK) and Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
3. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
4. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
5. The memory size of SPD Hub device is limited to 1024 Bytes. SPD Hub device ignores Blk Addr [4] bit.
6. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
7. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the SPD Hub may eventually ACK.
8. Figure 16 shows how the Host ends slave device operation.
9. For NVM read memory access (i.e. MemReg = 1), when last byte is reached (1024 Byte) or for volatile memory access (i.e. MemReg = 0), when last byte (i.e. MR255) is reached (extreme rare case), the slave device sends T = 0. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
10. Repeat Start or Repeat Start with 7'h7E.

Table 35. Read Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Notes 1, 3)	
Sr	1	0	1	0	HID			W = 0	A (Notes 2, 3, 4)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			R = 1	Blk Addr [4:1] (Note 5)				T	
	PEC								T	
Sr	1	0	1	0	HID			R = 1	A/N (Notes 6, 7)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1	
	PEC								T = 0 (Note 8)	Sr (Note 9) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK) and Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
3. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
4. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
5. The memory size of SPD Hub device is limited to 1024 Bytes. SPD Hub device ignores Blk Addr [4] bit.
6. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
7. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the SPD Hub may eventually ACK. The PEC calculation by the slave device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the slave device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
8. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
9. Repeat Start or Repeat Start with 7'h7E.

2.7.10.3 Default Read Address Pointer Mode

This mode works the same exact way as explained in Default Read Address Pointer Mode. Table 36 and Table 37 shows the read command data packet for PEC function disabled and enabled, respectively. When PEC function is enabled, MR18 [1] sets the number of bytes that Hub device sends out followed by the PEC calculation. If PEC is enabled, the host must complete the burst length as indicated in MR18 [1] register. In other words, the host must not interrupt the burst length prematurely for default address pointer read operation. The default read address pointer mode is only applicable to volatile register space (i.e. MemReg = 0).

Table 36. Read Command Data Packet with Read Address Pointer Mode; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			R = 1	A/N (Note 1)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1 (Notes 2, 3)	Sr (Note 4) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Figure 16 shows how the Host ends slave device operation.
3. When last byte (i.e. MR255) is reached (extreme rare case), the slave device sends T = 0. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 37. Read Command Data Packet with Read Address Pointer Mode; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			R = 1	A/N (Note 1)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1	
	PEC								T = 0 (Note 2)	Sr (Note 3) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Figure 17 shows how the slave device ends the operation followed by STOP operation
3. Repeat Start or Repeat Start with 7'h7E.

Table 38. Read CMD Data Packet with Read Address Pointer Mode and IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Notes 1, 2)	
Sr	1	0	1	0	HID			R = 1	A/N (Notes 2, 3)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1 (Notes 4, 5)	Sr (Note 6) or P

1. Figures 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
4. Figure 16 shows how the Host ends slave device operation.
5. When last byte (i.e. MR255) is reached (extreme rare case), the slave device sends T = 0. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
6. Repeat Start or Repeat Start with 7'h7E.

Table 39. Read CMD Data Packet with Read Address Pointer Mode and IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Notes 1, 2)	
Sr	1	0	1	0	HID			R = 1	A/N (Notes 2, 3)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1	
	PEC								T = 0 (Note 4)	Sr (Note 5) or P

1. Figures 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
4. Figure 17 shows how the slave device ends the operation followed by STOP operation
5. Repeat Start or Repeat Start with 7'h7E.

2.7.11 I3C Basic Slave Protocol - Host to Local Device (Through SPD5 Hub Device)

2.7.11.1 Write Operation - Data Packet

Table 40 to Table 45 shows examples write command data packet for different types of local devices behind the SPD5 Hub. These example do not show the optional IBI header byte that Host may choose to use. All local devices behind SPD5 Hub device also supports the IBI header byte similar to as shown in Table 30 and Table 31. See the device specific datasheet.

Table 40. Write Command Data Packet (e.g. TS); PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	Address [7:0]								T	
	Data								T	
	Data								T	
	...								T	
	Data								T	Sr (Note 4) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr; bit [7]).
2. The NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The TS device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 41. Write Command Data Packet (e.g. TS); PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	Address [7:0]								T	
	CMD			W = 0	0	0	0	0	T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr (Note 4) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
2. The NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The TS device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 42. Write Command Data Packet (e.g. PMIC); PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	0	1	HID			W = 0	A (Notes 1, 2, 3)	
	Address [7:0]								T	
	Data								T	
	Data								T	
	...								T	
	Data								T	Sr (Note 4) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
2. The NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The TS device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 43. Write Command Data Packet (e.g. PMIC); PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	0	1	HID			W = 0	A (Notes 1, 2, 3)	
	Address [7:0]								T	
	CMD			W = 0	0	0	0	0	T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr (Note 4) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions Repeat Start.
3. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 44. Write Command Data Packet (e.g. RCD); PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W = 0	A (Notes 1, 2, 3)	
	Data (I3C Bus Command)								T	
	Data (Byte Count = 8)								T	
	Data (Reserved; 0x00)								T	
	Data (Dev/Channel Num)								T	
	Data (Page Num [7:0])								T	
	Data (Reg Num [7:0])								T	
	Data (Wr Data [31:24])								T	
	Data (Wr Data [23:16])								T	
	Data (Wr Data [15:8])								T	
	Data (Wr Data [7:0])								T	Sr (Note 4) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Data, bit [7]).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The RCD device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 45. Write Command Data Packet (e.g. RCD); PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W = 0	A (Notes 1, 2, 3)	
	Data (I3C Bus Command)								T	
	Data (Byte Count = 8)								T	
	Data (Reserved; 0x00)								T	
	Data (Dev/Channel Num)								T	
	Data (Page Num [7:0])								T	
	Data (Reg Num [7:0])								T	
	Data (Wr Data [31:24])								T	
	Data (Wr Data [23:16])								T	
	Data (Wr Data [15:8])								T	
	Data (Wr Data [7:0])								T	
	Data (PEC [7:0])								T	Sr(Note 4) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Data, bit [7]).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The RCD device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

2.7.11.2 Read Operation - Data Packet

Table 46 to Table 51 shows examples read command data packet for different types of local devices behind the SPD5 Hub. These example do not show the optional IBI header byte that Host may choose to use. All local devices behind SPD5 Hub device also supports the IBI header byte similar to as shown in Table 34 and Table 35. Refer the device specific data sheet.

Table 46. Read Command Data Packet (e.g. TS); PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	Address [7:0]								T	
Sr	0	0	1	0	HID			R = 1	A/N (Notes 4, 5)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1 (Notes 6, 5)	Sr (Note 8) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The TS device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the device may eventually ACK.
5. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
6. Figure 16 shows how the Host ends slave device operation.
7. For volatile register access, when last byte (MR TBD from TS Spec) is reached (extreme rare case), the slave device sends T = 0. Figure 17 shows how the Host ends slave device operation.
8. Repeat Start or Repeat Start with 7'h7E.

Table 47. Read Command Data Packet (e.g. TS); PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	Address [7:0]								T	
	CMD			R = 1	0	0	0	0	T	
	PEC								T	
Sr	0	0	1	0	HID			R = 1	A/N (Notes 4, 5)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1	
	PEC								T = 0 (Note 6)	Sr (Note 7) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The TS device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the slave device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the slave device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
5. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
6. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
7. Repeat Start or Repeat Start with 7'h7E.

Table 48. Read Command Data Packet (e.g. PMIC); PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	0	1	HID			W = 0	A (Notes 1, 2, 3)	
	Address [7:0]								T	
Sr	1	0	0	1	HID			R = 1	A/N (Notes 4, 5)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1 (Notes 6, 7)	Sr (Note 8) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
4. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the device may eventually ACK.
5. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
6. Figure 16 shows how the Host ends slave device operation.
7. For volatile register access, when last byte is reached within the region (either Host region or DIMM Vendor region), it will continue to return the data but returned data is 0x00 if there is no valid password for DIMM vendor region or device vendor specific region. Once the address counter reaches R255, it resets to address R00 and it continues to return the data. Only Host can perform the STOP operation.
8. Repeat Start or Repeat Start with 7'h7E.

Table 49. Read Command Data Packet (e.g. PMIC); PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	0	1	HID			W = 0	A (Notes 1, 2, 3)	
	Address [7:0]								T	
	CMD			R = 1	0	0	0	0	T	
	PEC								T	
Sr	1	0	0	1	HID			R = 1	A/N (Notes 4, 5)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1	
	PEC								T = 0 (Note 6)	Sr (Note 7) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
4. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the slave device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the slave device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
5. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
6. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
7. Repeat Start or Repeat Start with 7'h7E.

The RCD device requires valid stable input clock (DCK_t, DCK_c), Reset _n and Chip Select input (DCS_n) to allow any read or write access on its I3C interface.

Table 50. Read Command Data Packet (e.g. RCD); PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W = 0	A (Notes 1, 2, 3)	
	Data (I3C Bus Command)								T	
	Data (Byte Count = 4)								T	
	Data (Reserved; 0x00)								T	
	Data (Dev/Channel Num)								T	
	Data (Page Num [7:0])								T	
	Data (Reg Num [7:0])								T	
Sr	1	0	1	1	HID			R = 1	A/N (Notes 4, 5)	
	Data (Byte Count)								T = 1	
	Data (Status)								T = 1	
	Data (Wr Data [31:24])								T = 1	
	Data (Wr Data [23:16])								T = 1	
	Data (Wr Data [15:8])								T = 1	
	Data (Wr Data [7:0])								T = 0 (Note 6)	Sr (Note 7) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Data).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The RCD device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the device may eventually ACK.
5. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
6. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
7. Repeat Start or Repeat Start with 7'h7E.

Table 51. Read Command Data Packet (e.g. RCD); PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W = 0	A (Notes 1, 2, 3)	
	Data (I3C Bus Command)								T	
	Data (Byte Count = 4)								T	
	Data (Reserved; 0x00)								T	
	Data (Dev/Channel Num)								T	
	Data (Page Num [7:0])								T	
	Data (Reg Num [7:0])								T	
	Data (PEC[7:0])								T	
Sr	1	0	1	1	HID			R = 1	A/N (Notes 4, 5)	
	Data (Byte Count)								T = 1	
	Data (Status)								T = 1	
	Data (Wr Data [31:24])								T = 1	
	Data (Wr Data [23:16])								T = 1	
	Data (Wr Data [15:8])								T = 1	
	Data (Wr Data [7:0])								T = 1	
	Data (PEC [7:0])								T = 0 (Note 6)	Sr (Note 7) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (1st bit of Data).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The RCD device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the slave device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the slave device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
5. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
6. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
7. Repeat Start or Repeat Start with 7'h7E.

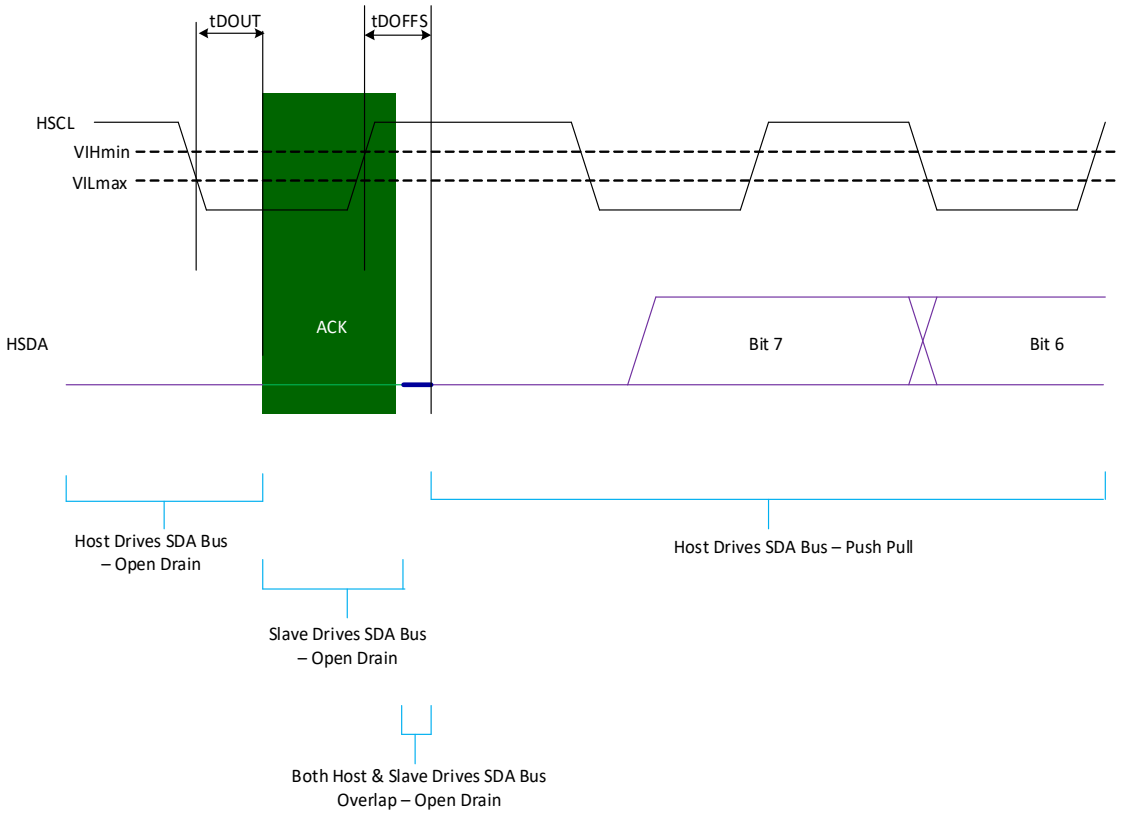


Figure 13. Slave Open Drain to Host Push Pull Hand Off Operation

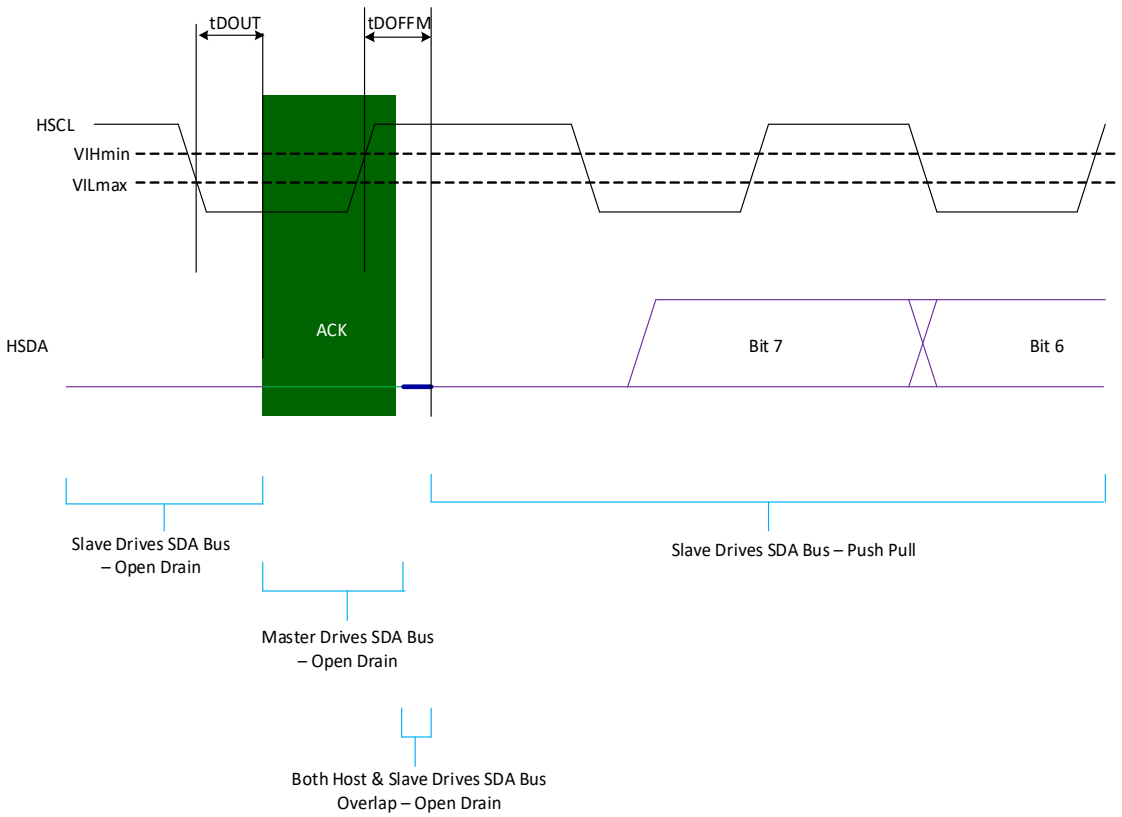


Figure 14. Master Open Drain (ACK) to Slave Push Pull Hand Off Operation

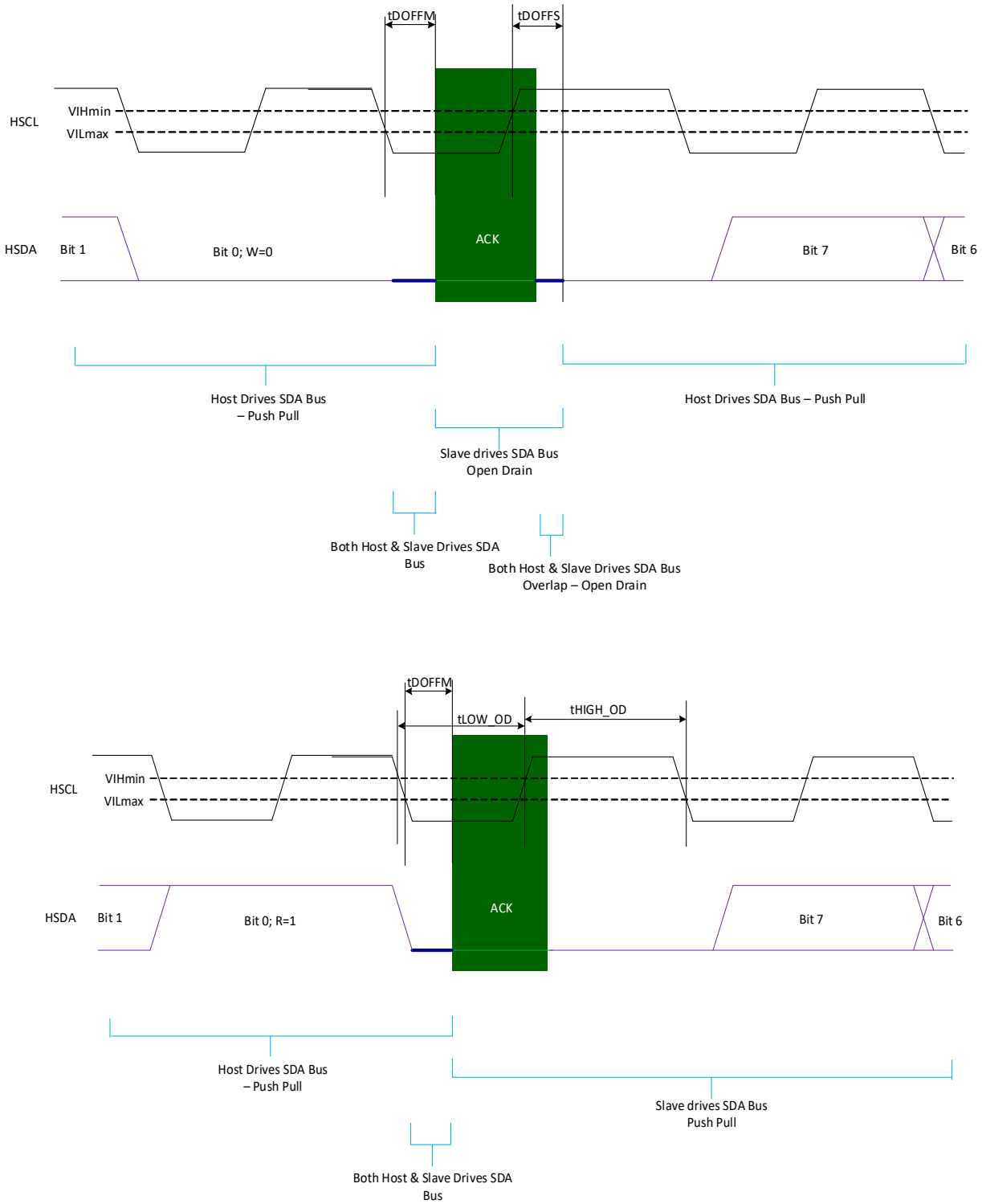


Figure 15. Master Push Pull to Slave Open Drain Hand Off Operation

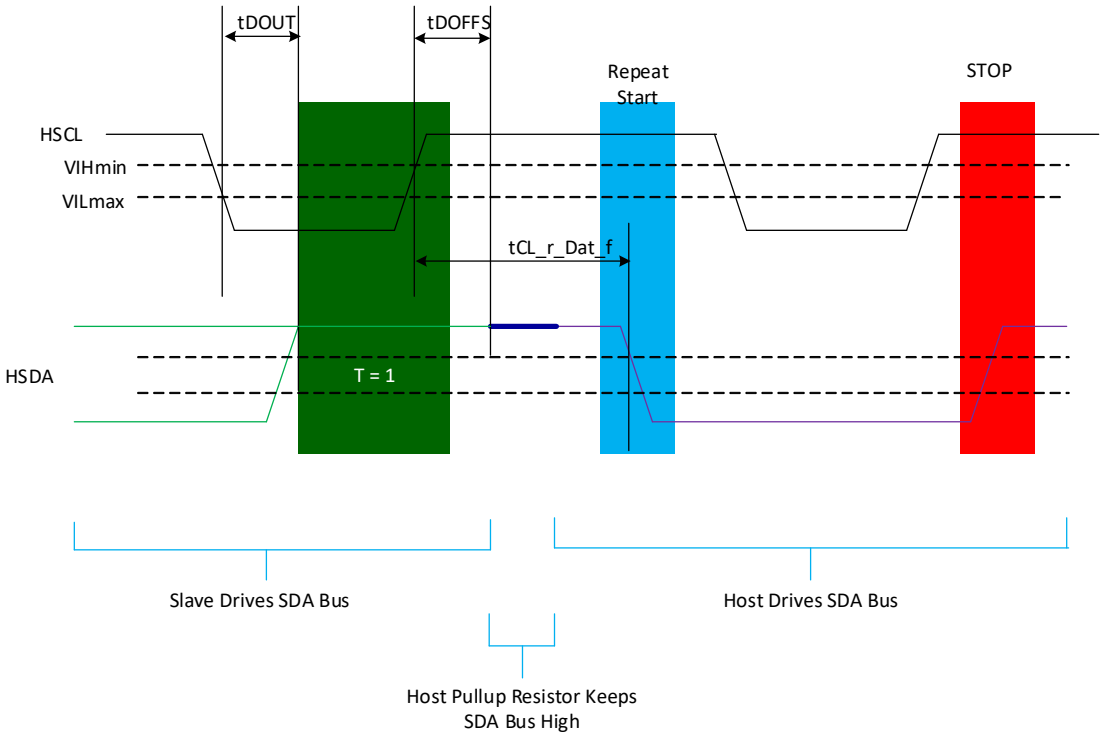


Figure 16. T = 1; Host Ends Read with Repeated START and STOP Waveform

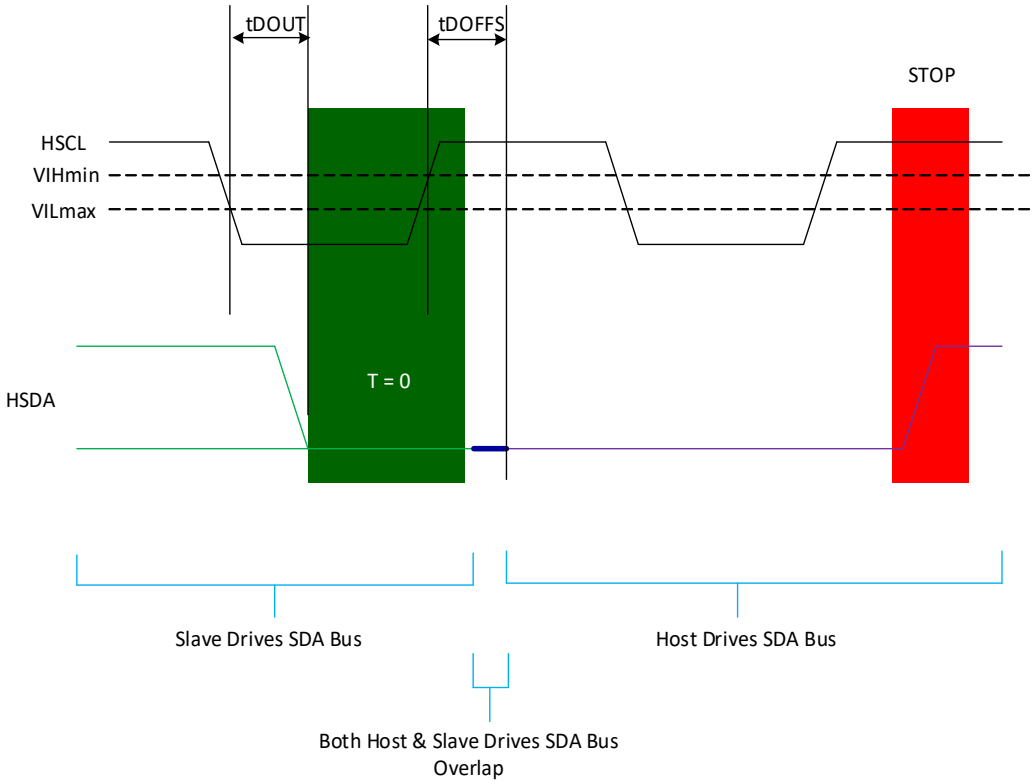


Figure 17. T = 0; Slave Ends Read; Host Generates STOP

2.7.12 In Band Interrupt (IBI)

In I^2C mode, in band interrupt function is not supported. Only I3C Basic mode supports in band interrupt function.

2.7.12.1 Enabling and Disabling In Band Event Interrupt Function

By default, all interrupt sources are disabled (i.e. set to 0). The host may enable following interrupts in the SPD5 Hub device. Once enabled, the SPD5 Hub device sends an IBI when that event occurs.

1. Error Interrupt Enable in MR27 [4]:
   a. When MR27 [4] = 1, the device sends the IBI at next available opportunity when any of the register bit in MR52 [7:5, 1:0] is set to 1 and sets MR48 [7] = 1 and updates Pending Interrupt Bits [3:0] = 0001 for GETSTATUS CCC.
   b. When MR27 [4] = 0, the device does not send the IBI regardless of the register bit status in MR52 [7:5, 1:0]. However, the device does set MR48 [7] = 1 and updates Pending Interrupt Bits [3:0] = 0001 for GETSTATUS CCC.
2. Temp Sensor Interrupt Enable in MR27 [3:0]: The host can set any combination of register bits to 1.
   a. When any of the register bits in MR27 [3:0] = 1 and if MR27 [4] = 1, the device sends the IBI at next available opportunity when the corresponding register bit in MR51 [3:0] is set to 1 and sets MR48 [7] = 1 and updates Pending Interrupt Bits [3:0] = 0001 for GETSTATUS CCC.
   b. When any of the register bits in MR27 [3:0] = 0 or MR27 [4] = 0, the device does not send the interrupt regardless of the corresponding register bit status in MR51 [3:0]. However, the device does set MR48 [7] = 1 and updates Pending Interrupt Bits [3:0] = 0001 for GETSTATUS CCC if any of the bits in MR27 [3:0] = 1 and MR27 [4] = 0.

2.7.12.2 Mechanics of Interrupt Generation - SPD5 Hub Device

Event interrupts may be generated by the SPD5 Hub device if IBI is enabled. When there is a pending interrupt (i.e.MR48 [7] = 1 and MR27 [4] = 1), the SPD5 Hub requests an interrupt after detecting START condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W = 1 on the SDA bus serially (synchronized by SCL falling transitions).

If the SPD5 Hub detects no START condition but if the Host to the SPD5 Hub device bus (HSDA and HSCL) has been inactive (no edges seen) for t_{AVAL} period, then the SPD5 Hub device may assert HSDA low by t_{IBI_ISSUE} time to request an interrupt. When the SPD5 Hub device requests an interrupt, the Host toggles the HSCL. The SPD5 Hub device transmits its 7-bit binary address; 1010 followed by 3 HID bits and then sets the R/W bit = 1.

When the SPD5 Hub device requests an interrupt, the host may take one of the following two actions:

- The Host sends ACK on 9th bit to accept the interrupt request. At this point, if the SPD5 Hub confirms that it has won the arbitration, the SPD5 Hub device transmits the IBI payload as shown in Table 52 and Table 53 for PEC disabled and PEC enabled configuration respectively. See Figure 18. Figure 18 just shows only first two data bits of the first payload byte (MDB Byte) to illustrate the timing. The interrupt payload contains MDB followed by MR51 and MR52 in order. The host then issues the STOP command. Note The timing waveform in Figure 18. The host then accepts the IBI payload if it sends an ACK on 9th bit to accept the interrupt request. The host can interrupt the IBI payload at T. If host stops the IBI payload at T bit in the middle of payload, the SPD5 Hub device retains the IBI status flag MR48 [7] = 1 and Pending Interrupt Bits [3:0] internally and waits for the next opportunity to request an interrupt. If the SPD5 Hub device successfully transmits the entire IBI payload, it then clears IBI status flag MR48 [7] = 0 and Pending Interrupt Bits [3:0] = 0000 on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.
- The Host sends NACK on the 9th bit as shown in Figure 19 followed by a STOP command. In this case, the SPD5 Hub device does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent an NACK, it does have a knowledge of which SPD5 Hub device sent the IBI request. The SPD5 Hub retains the IBI status flag MR48 [7] = 1 and Pending Interrupt Bits [3:0] = 0001.

Table 52. Hub IBI Payload Packet; PEC is Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1010				HID			R = 1	A (Note 1)	
	MDB = 0x00								T = 1	
	MR51 [7:0]								T = 1	
	MR52 [7:0]								T = 0 (Note 2)	P

1. Figure 14 shows how the transition occurs from Host Open Drain (ACK) to Slave Push Pull Operation (1st bit of MDB Byte bit [7]).
2. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.

Table 53. Hub IBI Payload Packet; PEC is Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1010				HID			R = 1	A (Note 1)	
	MDB = 0x00								T = 1	
	MR51 [7:0]								T = 1	
	MR52 [7:0]								T = 1	
	PEC								T = 0 (Note 2)	P

1. Figure 14 shows how the transition occurs from Host Open Drain (ACK) to Slave Push Pull Operation (1st bit of MDB Byte bit [7]).
2. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.

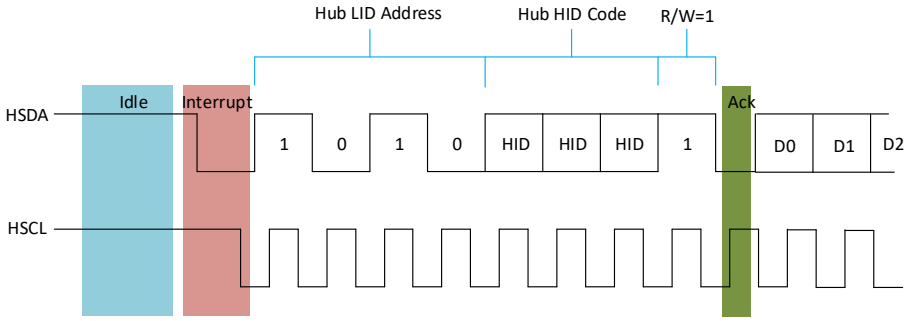


Figure 18. Hub Interrupt; Host Ack Followed by Hub Device IBI Payload

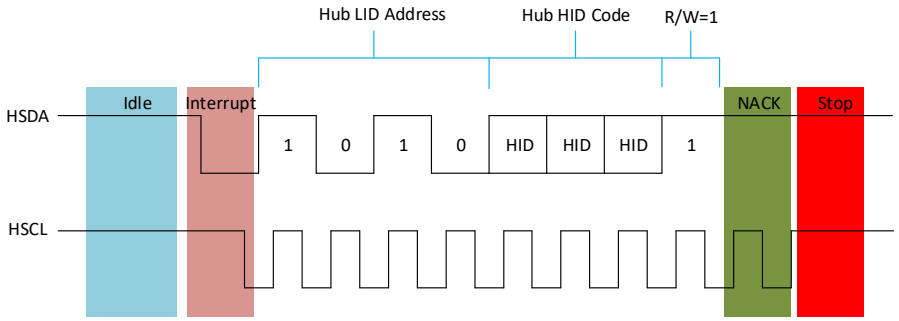


Figure 19. Hub Interrupt; Host NACK followed by STOP

2.7.12.3 Mechanics of Interrupt Generation - Local Slave Device

Event interrupts may be generated by the local device if IBI is enabled. When there is a pending interrupt in any local device and if IBI is enabled, the local device requests an interrupt after detecting START condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W = 1 on the SDA bus serially (synchronized by SCL falling transitions).

If the local device detects no START condition but if the Host to the local slave device (through the SPD5 Hub device) bus (LSDA and LSCL) has been inactive (no edges seen) for t_{AVAL} period, then any local device may assert LSDA low by t_{IBI_ISSUE} time to request an interrupt. When the local device requests an interrupt, the SPD5 Hub device propagates the LSDA to HSDA to Host. The Host toggles the HSCL. The local device transmits its 7-bit binary address (LID bits followed by HID bits) followed by R/W bit = 1 to the SPD5 Hub device. This is shown in Figure 20 top waveform.

The SPD5 Hub device forwards LID bits it receives from the local device to the Host. The SPD5 Hub device substitutes its own HID code in place of the HID bits it receives from the local device if SETHID CCC is not issued by Host and sends to the Host. This is shown in Figure 20 middle waveform. The SPD5 Hub device forwards HID bits it receives from the local device to the host if Host has issued SETHID CCC previously. This is shown in Figure 20 bottom waveform. The SPD5 Hub device forwards the R/W bit = 1 to the Host.

When the local device requests an interrupt, the host may take one of the following two actions:

- The Host sends ACK on 9th bit to accept the interrupt request. At this point, if the local device confirms that it has won the arbitration, the local device transmits the IBI payload as shown in Table 54 and Table 55 for PEC disabled and PEC enabled configuration respectively. See Figure 20. Figure 20 just shows only first two data bits of the first payload byte (MDB Byte) to illustrate the timing. The interrupt payload contains MDB Byte followed by appropriate slave device error register contents. The host then issues the STOP command. Note the timing waveform in Figure 20. The host then accepts the IBI payload if it sends an ACK on 9th bit to accept the interrupt request. The host can interrupt the IBI payload at T bit. If host stops the IBI payload at T bit in the middle of payload, the local device retains the IBI status flag and Pending Interrupt Bits [3:0] internally and waits for the next opportunity to request an interrupt. If the local device successfully transmits the entire IBI payload, it then clears IBI status flag and Pending Interrupt Bits [3:0] = 0000 on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.
- The Host sends NACK on the 9th bit as shown in Figure 21 followed by a STOP command. In this case, the local device does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent an NACK, it does have a knowledge of which local device sent the IBI request. The local device retains the IBI status flag and Pending Interrupt Bits [3:0] = 0001.

Table 54. Slave Device IBI Payload Packet; PEC is Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	LID				HID			R = 1	A (Note 1)	
	MDB = 0x00								T = 1	
	First Error Code Byte								T = 1	
	Second Error Code Byte								T = 1	
	...								T = 0 (Note 2)	P

1. Figure 14 shows how the transition occurs from Host Open Drain (ACK) to Slave Push Pull Operation (1st bit of Byte bit [7]).
2. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.

Table 55. Slave Device IBI Payload Packet; PEC is Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	LID				HID			R = 1	A (Note 1)	
	MDB = 0x00								T = 1	
	First Error Code Byte								T = 1	
	Second Error Code Byte								T = 1	
	...								T = 1	
	PEC								T = 0 (Note 2)	P

1. Figure 14 shows how the transition occurs from Host Open Drain (ACK) to Slave Push Pull Operation (1st bit of Byte bit [7]).
2. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.

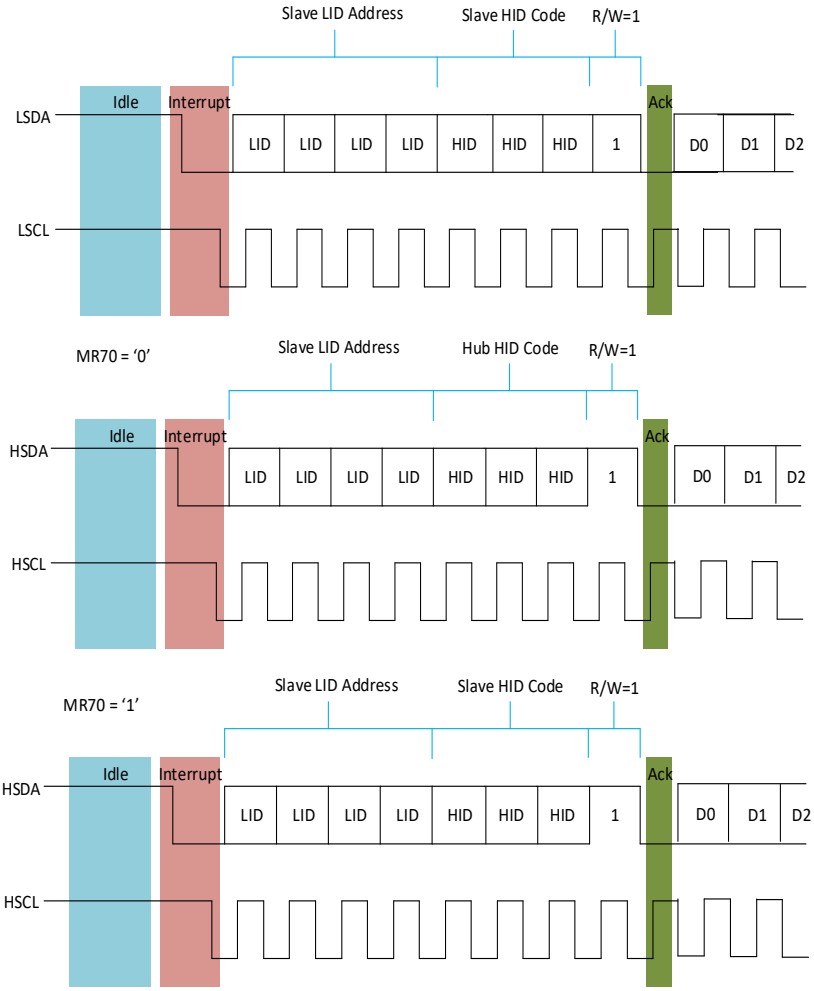


Figure 20. Local Device Interrupt, Host Ack Followed by Slave Device IBI Payload

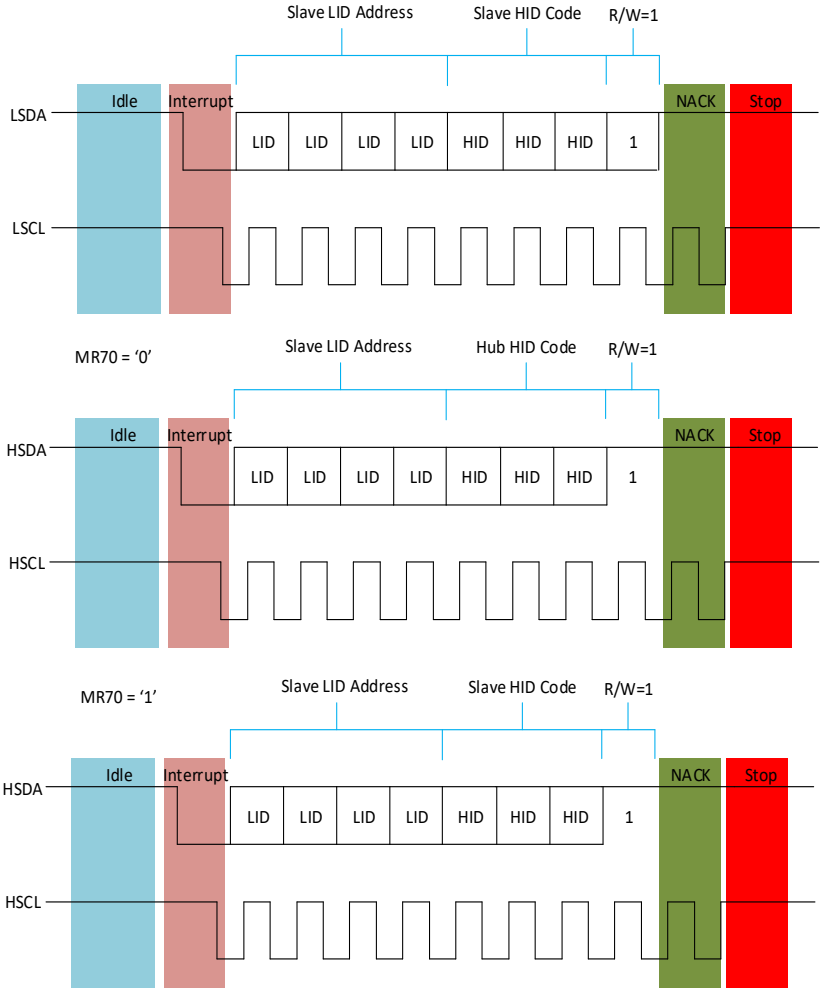


Figure 21. Local Device Interrupt; Host NACK Followed by STOP

2.7.12.4 Interrupt Arbitration; SETHID CCC is Not Issued By Host;

As there are multiple local slave devices behind the SPD5 Hub and there are multiple SPD5 Hub devices on I3C Basic bus, multiple device may request an interrupt when the I3C bus is inactive for t_{AVAL} period. Arbitration process is required.

Interrupt Arbitration - Among SPD5 Hub Devices

This section explains the interrupt arbitration among the SPD5 Hub devices only. There are up to 8 SPD5 Hub devices on the I3C bus.

As all SPD5 Hub devices have the same 4-bit LID code of 1010, the arbitration is always won by the lower HID code. For example, if one SPD5 Hub device has HID code of 000 and other SPD5 Hub device has a HID code of 011, through the arbitration process, the HID code of 000 wins. The SPD5 Hub device with a HID code of 011 must release the bus and wait for next opportunity to request an interrupt. Table 56 shows the arbitration priority based on the HID code for the SPD5 Hub device.

Table 56. Interrupt Arbitration - Among SPD5 Hub Devices

Hub Device LID Code	Hub Device HID Code	Arbitration Priority
1010	000	1
1010	001	2
1010	010	3
1010	011	4
1010	100	5
1010	101	6
1010	110	7
1010	111	8

Interrupt Arbitration - Among Local Slave Devices behind one SPD5 Hub Devices

This section explains the interrupt arbitration among the local devices only behind the SPD5 Hub. There are up to 14 local devices behind the SPD5 Hub.

As all local slave devices behind the SPD5 Hub devices have the same 3-bit HID code, Hence the arbitration is always won by the 4-bit LID code. For example, if one local slave device has LID code of 1001 and other local slave device has a LID code of 0010, through the arbitration process, the LID code of 0010 wins. The local device with a LID code of 1001 must release the bus and wait for next opportunity to request an interrupt. Table 57 shows the arbitration priority based on the LID code for the local devices. The Green color cells in Table 57 are the likely devices that will be on a standard DDR5 RDIMM or DDR5 LRDIMM. The Olive color cells in Table 57 do not apply.

During the interrupt arbitration phase, the SPD5 Hub device forwards the winning 4-bit LID code one digit at a time that it receives from the local slave devices to the Host.

The SPD5 Hub device discards the 3-bit 111 HID code received from the local slave device. Instead the SPD5 Hub device forwards its own unique 3-bit HID code one digit at a time to the host. As a result, the Host can identify the winning device based on the 4-bit LID code (Local slave device) and 3-bit HID code (the DIMM). Also, when the SPD5 Hub device substitutes its own unique 3-bit HID code to the host, its own receiver will see that at the input and it compares each 3 bits one at a time as it if the host sent those 3 bits. If there is a match, the SPD5 Hub device forwards 1 to the local device interface and if there is a mis-match, the SPD5 Hub device forward 0 to the local device interface. Because the local slave device sends 111 as its 3 bit HID code, the local device knows that it won the arbitration. See Figure 22.

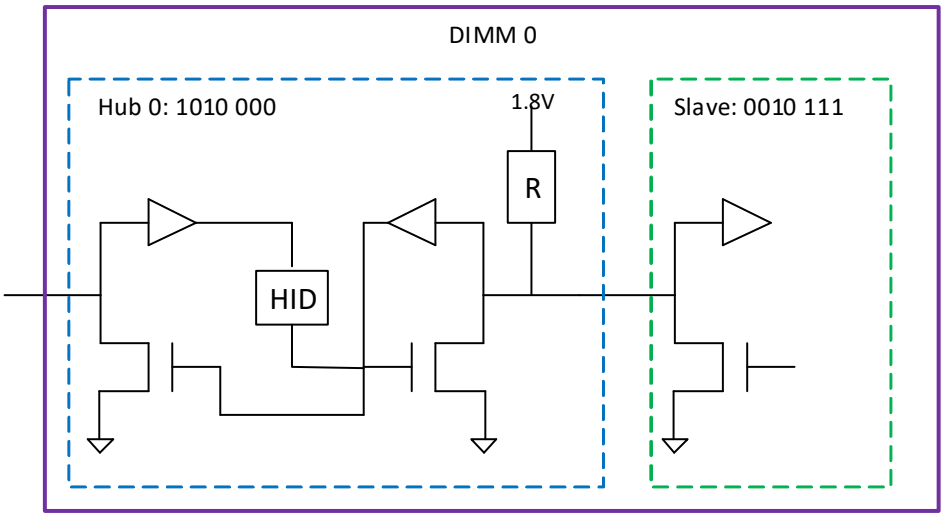


Figure 22. SPD5 Hub Function During Arbitration from Local Slave Device

Table 57. Interrupt Arbitration - Among Local Slave Devices

Device	Slave Device LID Code	Slave Device HID Code	Arbitration Priority
N/A	0000	N/A	N/A
RFU	0001	111	1
TS0	0010	111	2
RFU	0011	111	3
RFU	0100	111	4
RFU	0101	111	5
TS1	0110	111	6
RFU	0111	111	7
PMIC1	1000	111	8
PMIC0	1001	111	9
SPD Hub	1010	HID	N/A
RCD	1011	111	10
PMIC2	1100	111	11
RFU	1101	111	12
RFU	1110	111	13
N/A	1111	N/A	N/A

Interrupt Arbitration - Between SPD5 Hub Device and Local Slave Devices Behind the Hub

This section explains the interrupt arbitration among the SPD5 Hub device and all local devices behind that SPD5 Hub. There are up to 13 local devices behind each SPD5 Hub.

As the SPD5 Hub device LID code of 1010, any local slave devices with a lower LID code always wins the arbitration process as shown in Table 57. The local slave devices with a higher LID code than 1010, the SPD5 Hub device wins the arbitration process. As an example, for a typical DDR5 RDIMM/LRDIMM, the RCD always has the lowest priority for winning the interrupt arbitration.

Interrupt Arbitration - Among Local Slave Devices Behind Different SPD5 Hub Devices

This section explains the interrupt arbitration among the SPD5 Hub devices and all local devices behind any SPD5 Hub devices. There are up to 8 SPD5 Hub devices on the I3C bus and up to 13 local devices behind each SPD5 Hub.

The arbitration process is hybrid of Interrupt Arbitration - Among SPD5 Hub Devices section to Interrupt Arbitration - Between SPD5 Hub Device and Local Slave Devices Behind the Hub section. The device with the lowest 4-bit LID code across all local slave devices and across all SPD5 hub devices always wins the arbitration process. The HID code for that lowest LID code represents the SPD5 Hub device code.

The Table 58 shows four examples. In each example, the slave LID code column represent local slave device behind hub which has HID code value of 111; the Hub HID code column represents the SPD5 Hub device which has LID code of 1010 followed by its own unique HID code; the winning device column represent the final winner among all devices (either SPD Hub device or local slave devices) during the arbitration phase.

Example 1: There are total 5 devices (4 local slave devices and 1 Hub device) that are requesting an interrupt. These 5 devices are shown in the RED color text. The devices that are in the Black color text are not requesting an interrupt. The winning device is the local device LID code of 0010 and HID code of 111. This is because the LID code of 0010 is the lowest among three other local slave device code and its HID code is 111.

Example 2: There are total 4 devices (2 local slave devices and 2 Hub device) that are requesting an interrupt. These 4 devices are shown in the RED color text. The devices that are in the Black color text are not requesting

an interrupt. The winning device is the local device LID code of 1001 and HID code of 100. This is because the LID code of 1001 is the lowest among one other local slave device code and its HID code is 100.

Example 3: There are total of 3 devices (2 local slave devices and 1 Hub device) that are requesting an interrupt. These 3 devices are shown in the RED color text. The devices that are in Black color text are not requesting an interrupt. The wining device is the Hub device on DIMM0 with LID code of 1010 and HID code of 000. This is because LID code 1010 is lower than two other local slave device code and its HID code is 000.

Example 4: There are total of 2 devices (2 local slave devices) that are requesting an interrupt. These 2 devices are shown in RED color text. The devices that are in Black color text are not requesting an interrupt. This example is unique as two identical slave devices across two different DIMM device is requesting an interrupt. The winning device is the local slave device on DIMM 0 with LID code of 0010 and DIMM 0 HID code of 000. This is because DIMM0 HID code 000 is lower than DIMM2 HID code of 010. See Figure 23 and also the Interrupt Arbitration - Among Local Slave Devices behind one SPD5 Hub Devices section.

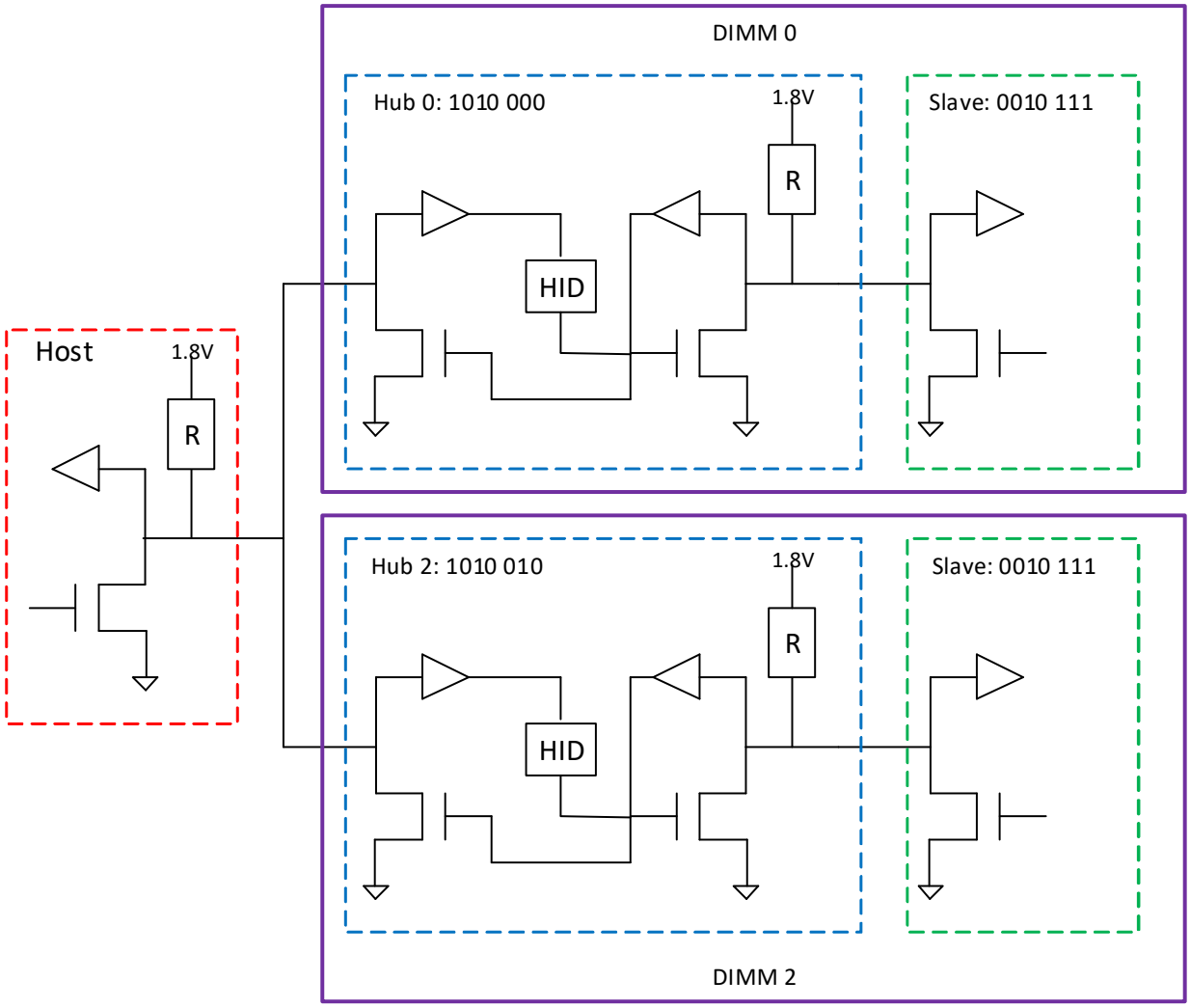


Figure 23. Arbitration Between Two Local Identical Slave Devices

Table 58. Interrupt Arbitration - Among Local Slave and SPD5 Hub Devices

Example 1			Example 2			Example 3			Example 4		
Slave LID Code	Hub HID Code	Winning Device	Slave LID Code	Hub HID Code	Winning Device	Slave LID Code	Hub HID Code	Winning Device	Slave LID Code	Hub HID Code	Winning Device
0010 0110 1001 1011	000		0010 0110 1001 1011	000		0010 0110 1001 1011	000	1010 000	0010 0110 1001 1011	000	0010 000
0010 0110 1001 1011	001		0010 0110 1001 1011	001		0010 0110 1001 1011	001		0010 0110 1001 1011	001	
0010 0110 1001 1011	010		0010 0110 1001 1011	010		0010 0110 1001 1011	010		0010 0110 1001 1011	010	
0010 0110 1001 1011	011		0010 0110 1001 1011	011		0010 0110 1001 1011	011		0010 0110 1001 1011	011	
0010 0110 1001 1011	100		0010 0110 1001 1011	100	1001 100	0010 0110 1001 1011	100		0010 0110 1001 1011	100	
0010 0110 1001 1011	101		0010 0110 1001 1011	101		0010 0110 1001 1011	101		0010 0110 1001 1011	101	
0010 0110 1001 1011	110		0010 0110 1001 1011	110		0010 0110 1001 1011	110		0010 0110 1001 1011	110	
0010 0110 1001 1011	111	0010 111	0010 0110 1001 1011	111		0010 0110 1001 1011	111		0010 0110 1001 1011	111	

Interrupt Arbitration - Between Host and Any Hub or Any Local Slave Devices Behind Hub

When the bus is idle for t_{AVAL} time, any Hub device or any local device behind the Hub can request an interrupt by pulling the SDA bus low.

In an uncommon but possible scenario would be that at the exact same time as when the Hub or local slave devices are requesting an interrupt, the host is starting an operation to the hub or local slave devices. When this happens, Host also gets involved in the arbitration process along with the Hub or the local slave devices. During the arbitration phase, there will be always only one winning device and it could be either Hub or the local slave device or the Host.

If the host wins during the arbitration phase, it continues with normal operation. The losing Hub or local slave device waits for next opportunity to send an interrupt.

If the host loose during the arbitration phase, it host must let go of the bus. When Host looses during the arbitration, the host must let the Hub or local slave device finish sending their 4-bit LID code followed by 3-bit HID code followed by R/W = 1. At this point, during the 9th bit, the host has two options to take the action as follows:

- Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning Hub or local slave device. After the IBI payload, the host issues STOP operation.
- Host sends an NACK followed by STOP operation.

In a rare but still possible scenario would be that at the exact same time as when the Hub or local slave device is requesting an interrupt, the host is starting an operation to that same exact hub or local slave devices. When this happens, neither Host or nor the hub or local slave device knows it is a winner until the 8th bit and Host always wins. This is because, the hub or local slave device sends R = 1 (8th bit) during the interrupt. The host sets W = 0 (8th bit) during the operation. As a result, the host wins and the hub or slave device must let go of the bus and wait for the next opportunity to send an interrupt. This is shown as example 3 in Table 59.

The Table 59 shows three examples. In each example, the Host is targeting an operation to the device cod. The slave LID code column represent local slave device behind hub which has HID code value of 111; the Hub HID code column represents the SPD5 Hub device which has LID code of 1010 followed by its own unique HID code; the winning device column represent the final winner among all devices (either Host or SPD Hub device or local slave devices) during the arbitration phase.

In example 1, there are total of 5 devices (1 Hub device and 4 local slave devices) are requesting an interrupt at exactly same time as when the Host is starting an operation to hub device on DIMM 3 (1010 011). The winning device is local slave device 0010 111 because it has the lower 4-bit LID code.

In example 2, there are total of 4 devices (2 Hub devices 2 local slave devices) are requesting an interrupt at exactly same time as when the Host is requesting an operation to the local slave device on DIMM5 (0110 101). The host is the winner because its intended target device has the lower 4-bit LID code than devices that are requesting an interrupt.

In example 3, there are is one 1 hub device on DIMM 2 is requesting an interrupt at exactly the same time as when Host is requesting an operation to the same exact Hub device on DIMM2. In this case, the host is the winner because the 8-bit will be driven low by the Host (W = 0) while the Hub device drives it high (R = 1) during the interrupt.

In an extreme rare but still possible scenario would be that at the exact same time as when the Hub or local slave device is requesting an interrupt, the host is requesting a read operation with default read address pointer mode to the same exact hub or local slave device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the hub or local slave device sends R = 1 (8th bit) during the interrupt and Host also sends R = 1 for read request with default read address pointer mode. As a result, there is no winner because all devices, i.e. the Host or the hub or the local slave device, is waiting for other device to ACK. In this case, no device will ACK. Since there is no ACK by any device, the Host must time out and repeats the read request with Repeat Start. When it repeats the read request with Repeat Start, the hub or local slave device does not send an interrupt because it sees Repeat Start.

Table 59. Interrupt Arbitration -Best Host and Local Slave and SPD5 Hub Devices

Example 1				Example 2				Example 3			
Host Target Device	Slave LID Code	HubHID Code	Winning Device	Host Target Device	Slave LID Code	Hub HID Code	Winning Device	Host Target Device	Slave LID Code	Hub HID Code	Winning Device
1010 011	0010 0110 1001 1011	000		0110 101	0010 0110 1001 1011	000		1010 010	0010 0110 1001 1011	000	
	0010 0110 1001 1011	001			0010 0110 1001 1011	001			0010 0110 1001 1011	001	
	0010 0110 1001 1011	010			0010 0110 1001 1011	010			0010 0110 1001 1011	010	Host operation to 1010 010
	0010 0110 1001 1011	011			0010 0110 1001 1011	011			0010 0110 1001 1011	011	
	0010 0110 1001 1011	100			0010 0110 1001 1011	100			0010 0110 1001 1011	100	
	0010 0110 1001 1011	101			0010 0110 1001 1011	101	Host operation to 0110 101		0010 0110 1001 1011	101	
	0010 0110 1001 1011	110			0010 0110 1001 1011	110			0010 0110 1001 1011	110	
	0010 0110 1001 1011	111	0010 111		0010 0110 1001 1011	111			0010 0110 1001 1011	111	

2.7.12.5 Interrupt Arbitration; SETHID CCC is Issued by Host;

The interrupt arbitration process works similar way as defined in Interrupt Arbitration; SETHID CCC is Not Issued By Host; but with a simplification. It is assumed that in this case, the all slave devices behind the Hub across all DIMMs on I3C Basic bus has a unique 7-bit device select code. Further, it assumes that all devices on a DIMM has the same 3-bit HID code.

The SPD5 Hub device forwards the 4-bit LID code and 3-bit HID code one digit at a time that it receives from the local slave devices to the Host. The SPD5 Hub device's own receiver will see the same input and it forwards it back to the local device interface.

Interrupt Arbitration - Between SPD5 Hub Device and Local Slave Devices behind Hub

On an any given DIMM, the arbitration is always won by the device that has the lowest 4-bit LID code since all devices on the DIMM has same 3-bit HID code.

Interrupt Arbitration - Between all SPD5 Hub Devices and All Local Slave Devices behind Hub

Across multiple DIMMs, the arbitration is always won by the device that has the lowest 7-bit address (4-bit LID + 3-bit HID).

Interrupt Arbitration - Between Host and All Devices

In an uncommon but possible scenario would be that at the exact same time as when the slave device is requesting an interrupt, the host is starting an operation to the slave device. When this happens, Host also gets involved in the arbitration process along with the slave devices. During the arbitration phase, there will be always only one winning device and it could be either Host or the slave device.

If the host wins during the arbitration phase, it continues with normal operation. The losing slave device waits for next opportunity to send an interrupt.

If the host lose during the arbitration phase, it host must let go of the bus. When Host looses during the arbitration, the host must let the slave device finish sending their 4-bit LID code followed by 3-bit HID code followed by R/W = 1. At this point, during the 9th bit, the host has two options to take the action as noted:

- Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning slave device. After the IBI payload, the host issues STOP operation.
- Host sends an NACK followed by STOP operation.

In a rare but still possible scenario would be that at the exact same time as when the SPD5 Hub device is requesting an interrupt, the host is starting an operation to that same SPD5 Hub device. When this happens, neither Host or nor the SPD5 Hub device knows it is a winner until the 8th bit and Host always wins. This is because, the SPD5 hub device sends R = 1 (8th bit) during the interrupt. The host sets W = 0 (8th bit) during the operation. As a result, the host wins and the SPD5 Hub device must let go of the bus and wait for the next opportunity to send an interrupt.

In an extreme rare but still possible scenario would be that at the exact same time as when the SPD5 Hub device is requesting an interrupt, the host is requesting a read operation with default read address pointer mode to the SPD5 Hub device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the SPD5 Hub device sends R = 1 (8th bit) during the interrupt and Host also sends R = 1 for read request with default read address pointer mode. As a result, there is no winner because all devices, i.e. the Host or the SPD5 Hub device, is waiting for other device to ACK. In this case, no device will ACK. Since there is no ACK by any device, the Host must time out and repeats the read request with Repeat Start. When it repeats the read request with Repeat Start, the SPD5 Hub device does not send an interrupt because it sees Repeat Start.

2.7.12.6 Clearing Device Status and IBI Status Registers

The SPD5 Hub device provides the IBI status in MR48 [7] by setting it to 1. The SPD5 Hub device clears the IBI status register MR48 [7] to 0 automatically when it sends a complete IBI (including payload and without interruption) and it also clears Pending Interrupt Bits [3:0] to 0000. Once IBI status register is cleared, the SPD5 Hub does not request for an IBI again unless another event occurs.

The SPD5 Hub device provides the device status in MR51 and MR52 registers. The status information in MR51 and MR52 are latched and remains set even after the SPD5 Hub device sends IBI payload and clears the IBI status register MR48 [7] to 0. The host must explicitly clear the status register through Clear command by writing 1 for appropriate status or by issuing a Global clear command.

After Host issues clear command, if the condition is no longer present, the SPD5 Hub device clears the appropriate status register, clears the IBI status register to 0 and Pending Interrupt Bits [3:0] to 0000 even if the SPD5 Hub device has not sent the IBI. After Host issues clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to 1 and Pending Interrupt Bits [3:0] to 0001 even if the device has already sent the IBI and entire IBI payload.

2.7.13 Packet Error Check (PEC) Function

In I^{2}C mode, packet error checking is not supported. Only I3C Basic mode supports packet error checking.

The SPD5 Hub device implements an 8-bit Packet Error Code (PEC) which is appended at the end of all transactions if PECs is enabled through DEVCTRL CCC or by directly writing 1 to MR18 [7]. The PEC is a CRC-8

value calculated on all the messages bytes except for START, REPEATED START, STOP conditions or T-bits, ACK and NACK and IBI header (7'h7E followed by W = 0) bits.

The polynomial for CRC-8 calculations is:

- $C(X) = X^8 + X^2 + X^1 + 1$

The seed value for PEC function is all zero.

When Host calculates PEC for SPD5 Hub device, it includes LID and HID bits followed by R/W bit.

2.7.14 Parity Error Check Function

In I^2C mode, parity error checking is not supported except for supported CCCs. Only I3C Basic mode supports parity error checking.

By default, when SPD5 device is put in I3C Basic mode, parity function is automatically enabled. The host can disable the function after it is enabled. Host can also disable the parity function with DEVCTRL CCC or by directly writing 1 to MR18 [6]. When parity function is disabled, the SPD5 device simply ignores the T bit information from the Host. The host may actually choose to compute the parity and send that information during T bit or simply drive static low or high in T bit.

The SPD5 device implements ODD parity. If an odd number of bits in the byte are 1, the parity bit value is 0. If even number of bits in the byte are 1, the parity bit value is 1. The host computes the parity and sends during T bit.

2.7.15 Packet Error Check and Parity Error Handling

There are two types of error checking done by the SPD5 Hub device. Parity error checking and Packet Error checking. By default, the parity error checking is always enabled and packet error checking is disabled when the SPD5 Hub device is put in I3C Basic mode. The host may enable the packet error checking at any time. The parity error is calculated for each byte. The host sends parity error information in T bit.

I3C basic defines S0, S1, S2, S3, S4, S5, S6 error detection for slave devices. Only S1 and S2 error detection is supported by the SPD5 Hub for parity checking. All other errors are not supported and not applicable.

2.7.15.1 Write Command Data Packet Error Handling - PEC Disabled

The SPD5 Hub device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host as shown in Table 60.

Table 60. Write Command Data Packet; PEC Disabled

tart	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] (Note 4)				T	
	Data								T	
	...								T	
	Data								T	Sr (Note 5) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD Hub device ignores Blk Addr [4] bit.
5. Repeat Start or Repeat Start with 7'h7E.

Write command - if no parity error:

- The SPD5 Hub device executes the command.

Write command - if parity error:

- The SPD5 Hub device discards the byte in the packet that had a parity error.
- The SPD5 Hub device discards all subsequent bytes in that packet until the STOP operation. The SPD5 Hub device may or may not check parity for all sub-sequent bytes in that packet.
- Note that as the packet contains more than one byte, if first byte had no parity error but the second byte had a parity error, the SPD5 Hub device may or may not execute the first byte operation but second byte and all subsequent bytes operations are discarded.
- The SPD5 Hub device sets the MR52 [0], MR48 [7] and P_Err in GETSTATUS CCC to 1; updates Pending Interrupt Bits [3:0] to 0001 and waits for the next opportunity to send an in band interrupt if IBI is enabled.

2.7.15.2 Read Command Data Packet Error Handling - PEC Disabled

The SPD5 Hub device checks for parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in Table 61.

The SPD5 Hub device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes that SPD5 Hub device sends. The SPD5 Hub device sends Continuous (1) or Stop (0) information during T bit.

Table 61. Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] (Note 4)				T	
Sr	1	0	1	0	HID			R = 1	A/N (Notes 5, 6)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1 (Notes 7, 6)	Sr (Note 9) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD Hub device ignores Blk Addr [4] bit.
5. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the device may eventually ACK.
6. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
7. Figure 16 shows how the Host ends slave device operation.
8. For NVM memory access (i.e. MemReg = 1), when last byte is reached within 16 byte boundary or for volatile memory access (i.e. MemReg = 0), when last byte (i.e. MR 255) is reached (extreme rare case), the slave device sends T = 0. Figure 17 shows how the Host ends slave device operation.
9. Repeat Start or Repeat Start with 7'h7E.

Read Command - If no parity error:

- The SPD5 Hub sends ACK back to the host when Host perform Start Repeat operation.
- The SPD5 Hub device executes the command and sends the data as shown in Table 61.

Read Command - If parity error:

- The SPD5 Hub device discards the byte in the packet that had a parity error.
- The SPD5 Hub device discards second byte in that packet if the parity error occurred in first byte. The SPD5 Hub device may or may not check the parity for second byte in that packet.
- The SPD5 Hub sends NACK back to the host when Host performs a Start Repeat operation. This is shown in the RED color cell in Table 61. The NACK represents either a parity error in one of the two bytes or that SPD5 Hub is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times as it may desire. If the SPD5 Hub device NACKs due to parity error in a previous byte from the host, it will always NACK regardless of how many times host tries Repeat Start.
- The SPD5 Hub does not send the data shown in Table 61 and instead expects Host to perform STOP operation.
- The SPD5 Hub device sets MR52 [0] and MR48 [7] and P_Err in GETSTATUS CCC to 1; updates Pending Interrupt Bits [3:0] to 0001 and waits for the next opportunity to send an in band interrupt if IBI is enabled.

2.7.15.3 Write Command Data Packet Error Handling - PEC Enabled

The SPD5 Hub device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host as shown in Table 62. Further, the SPD5 Hub device checks for the packet error for the entire packet (from Start condition until last byte of Data) that it receives from the host as shown in Table 62.

Table 62. Write Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			W = 0	Blk Addr [4:1] (Note 4)				T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr (Note 5) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity or PEC errors in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD Hub device ignores Blk Addr [4] bit.
5. Repeat Start or Repeat Start with 7'h7E.

Write command - if no parity error:

- The SPD5 Hub device waits for the entire packet. If no error in packet, the SPD5 Hub device executes the command. If there is an error in the packet, the SPD5 Hub device discards the entire packet and does not execute that packet and waits for STOP, sets the MR52 [1] and MR48 [7] to 1 and PEC_Err in GETSTATUS CCC to 1; updates Pending Interrupt Bits [3:0] to 0001 in GETSTATUS CCC and waits for the next opportunity to send in band interrupt if IBI is enabled.

Write command - if parity error:

- The SPD5 Hub device discards that byte and the entire packet until STOP operation.

- The SPD5 Hub device sets MR52 [0] and MR48 [7] and P_Err in GETSTATUS CCC to 1; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to 0001 and waits for the next opportunity to send in band interrupt if IBI is enabled.
- The SPD5 Hub device may or may not check the error for the packet. If the SPD5 Hub device checks for the packet error, likely it will detect an error in the packet and the device may also set MR52 [1] and PEC_Err in GETSTATUS CCC to 1 as well.

2.7.15.4 Read Command Data Packet Error Handling - PEC Enabled

The SPD5 Hub device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in Table 63.

The SPD5 Hub device does not compute the parity when it sends the data to the Host. The does not check for parity error for the bytes shown in Table 63. The SPD5 Hub device sends Continuous (1) or Stop (0) information during T bit when SPD5 Hub device is sending the read data.

The SPD5 Hub device checks for the PEC error for a packet that it receives from the Host from Start condition to Repeat Start condition (from first device select code followed by the address offset and CMD byte).

The SPD5 Hub device computes the packet error code for the entire packet starting with Repeat Start (device select code and the data SPD5 Hub device transmits back to Host)

Table 63. Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W = 0	A (Notes 1, 2, 3)	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			R = 1	Blk Addr [4:1] (Note 4)				T	
	PEC								T	
Sr	1	0	1	0	HID			R = 1	A/N (Notes 5, 6)	
	Data								T = 1	
	...								T = 1	
	Data								T = 1	
	PEC								T = 0 (Note 7)	Sr (Note 8) or P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity or PEC errors in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
5. If slave device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as required. If slave device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the slave device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the slave device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
6. Figure 15 shows how the transition occurs from Host Push Pull Operation to Slave Open Drain (ACK).
7. Figure 17 shows how the slave device ends the operation followed by Host STOP operation.
8. Repeat Start or Repeat Start with 7'h7E.

Read command - If no parity error and no PEC error:

- The SPD5 Hub sends ACK back to the host when Host perform a Start Repeat operation.
- The SPD5 Hub device executes the command and sends the data as shown in Table 63.
- The SPD5 Hub computes PEC for the bytes shown in Table 63.

Read command - if parity error or PEC error:

- The SPD5 Hub device discards the byte in the packet that had a parity error.
- The SPD5 Hub device discards second byte in that packet if a parity error occurred in first byte. The SPD5 Hub device may or may not check parity for the second byte in that packet.
- The SPD5 Hub device discards the packet if there is a PEC error.
- The SPD5 Hub sends NACK back to the host when Host perform Start Repeat operation. This is shown in the RED color cell in Table 63. The NACK represents either PEC error or a parity error in one of the three bytes or that SPD5 Hub is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times as required. The PEC calculation by SPD5 Hub device only includes device select code of the ACK responses of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the SPD5 Hub device includes the device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and other NACK responses of the device select codes of the Repeat Start are not included in PEC calculation. If the SPD5 Hub device NACKs due to PEC error or a parity error in a previous bytes from Host, it will always NACK regardless of how many times Host tries Repeat Start.
- The SPD5 Hub does not send any data shown in Table 63 and instead expects Host to perform STOP operation.
- The SPD5 Hub device sets MR52 [0] and MR48 [7] and P_Err in GESTATUS CCC to 1 for parity error and MR52 [1] and MR48 [7] and PEC_Err in GETSTATUS CCC to 1 for PEC error. Further, the SPD5 Hub updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to 0001 and waits for the next opportunity to send an in band interrupt if IBI is enabled.

2.7.16 CCC Packet Error Handling

Parity error and PEC error detected in a CCC packet are handled the same way as described for normal Read/Write operation.

2.7.17 Error Reporting

All error conditions including PEC error check and Parity error check detected by the SPD5 Hub devices are captured in MR52 registers.

There are three different possible ways error information can be communicated to the host.

1. The Host makes the read request to MR51 and MR52 registers.
2. The Host starts any transaction with 7'h7E IBI header. (Only applicable in I3C Basic Mode)
3. The SPD5 Hub device sends in band interrupt if enabled, when its SCL and SDA input has been idle for t_{AVAL} time. (Only applicable in I3C Basic Mode).

2.7.18 I3C Basic Common Command Codes (CCC)

The I3C Basic spec lists large number of Common Command Codes (CCC). Not all CCC are required to be supported. The SPD5 Hub device NACKs for all unsupported CCC. The SPD5 Hub supports CCC as listed in Table 64.

The SPD5 Hub device requires STOP operation in between when switching from CCC operation to private device specific Write or Read or Default Read Address Pointer mode operation and vice versa. In other words, any CCC operation must be followed by STOP operation before continuing to any device specific Write or Read or Default Read Address Pointer mode operation. Similarly, any device specific Write or Read or Default Read Address

Pointer mode operation must be followed by STOP operation before continuing to any CCC operation. The SPD5 Hub device also requires STOP operation between any direct CCC to broadcast CCC.

The SPD5 Hub device does allow Repeat Start operation between any direct CCC to any other direct CCC or between any broadcast CCC to any other broadcast CCC or between any private Write or Read or Default Read Address Pointer mode operation to any other private Write or Read or Default Read Address Pointer mode operation.

Table 64. SPD5 Hub CCC Support Requirement

CCC	Mode	Code	Description	Note
ENEC	Broadcast	0x00	Enable Event Interrupts	
	Direct	0x80		
DISEC	Broadcast	0x01	Disable Event Interrupts	
	Direct	0x81		
RSTDAA	Broadcast	0x06	Put the device in I^2C Mode (aka: Reset Dynamic Address Assignment)	
	Direct	0x86		
SETAASA	Broadcast	0x29	Put the device in I3C Basic Mode (aka: Set All Addresses to Static Address)	
GETSTATUS	Direct	0x90	Get Device Status	
DEVCAP	Direct	0xE0	Get Device Capability	
SETHID	Broadcast	0x61	SPD Hub updates 3-bit HID field, updates T bit with updated parity calculation for all devices behind Hub and stops 3-bit HID translation	
DEVCTRL	Broadcast	0x62	Configure SPD Hub and all devices behind Hub	

2.7.18.1 ENEC CCC

The ENEC CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. When ENEC CCC is registered by the SPD5 Hub, it updates MR27 [4] = 1 and it takes in effect at the next Start operation (i.e. after STOP operation). Table 65 to Table 68 shows an example of a single ENEC CCC. Table 69 shows the encoding definition for ENEC CCC.

In I3C Basic mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 65. ENEC CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	Sr (Note 2) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 66. ENEC CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	
	PEC								T	Sr (Note 2) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 67. ENEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x80 (Direct)								T	
Sr	DevID[6:0]							W = 0	A (Notes 1, 2)	
	0x00							ENINT	T	Sr (Note 3) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 68. ENEC CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x80 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W = 0	A (Notes 1, 2)	
	0x00							ENINT	T	
	PEC								T	Sr (Note 3) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 69. ENEC CCC Byte Encoding

Bit	Encoding	Notes
ENINT	0 = No Action 1 = Enable IBI Interrupt	It is illegal for Host to issue ENEC CCC with ENINT bit = 0

2.7.18.2 DISEC CCC

The DISEC CCC is only supported after device is put in I3C mode. In I^2C mode, it is illegal for host to issue this CCC. When DISEC CCC is registered by the SPD5 Hub, it updates MR27 [4] = 0 and it takes in effect at the next Start operation (i.e. after STOP operation). Table 70 to Table 73 shows an example of a single DISEC CCC. Table 74 shows the encoding definition for DISEC CCC.

In I3C Basic mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 70. DISEC CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	Sr (Note 2) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 71. DISEC CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	
	PEC								T	Sr (Note 2) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 72. DISEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x81 (Direct)								T	
Sr	DevID[6:0]							W = 0	A (Notes 1, 2)	
	0x00							DISINT	T	Sr (Note 3) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 73. DISEC CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x81 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W = 0	A (Notes 1, 2)	
	0x00							DISINT	T	
	PEC								T	Sr (Note 3) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 74. DISEC CCC Byte Encoding

Bit	Encoding	Notes
DISINT	0 = No Action 1 = Disable IBI Interrupt	It is illegal for Host to issue DISEC CCC with DISINT bit = 0

2.7.18.3 RSTDAA CCC

The RSTDAA CCC is only supported after device is put in I3C mode. In I^2C mode, this CCC is ignored. When RSTDAA CCC is registered by the SPD5 Hub, it updates MR18 [5] = 0 and INF_SEL bit in GETSTATUS CCC to 0. Further it disables IBI and PEC function (MR27 [4] = 0, MR18 [7] = 0 respectively) and clears parity function MR18 [6] = 0) and it takes in effect at the next Start operation (i.e. after STOP operation).

Table 75 to Table 78 shows an example of a single RSTDAA CCC.

In I3C Basic mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 75. RSTDAA CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x06 (Broadcast)								T	P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

Table 76. RSTDAA CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x06 (Broadcast)								T	
	PEC								T	P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

Table 77. RSTDAA CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x86 (Direct)								T	
Sr	DevID[6:0]							W = 0	A (Notes 1, 2)	P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.

Table 78. RSTDAA CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x86 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W = 0	A (Notes 1, 2)	
	PEC								T	P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.

2.7.18.4 SETAASA CCC

The SETAASA CCC is only supported when device is in I^2C mode. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any parity error and to avoid subsequent undesired implication, the host shall limit the maximum speed of operation for this CCC to 4MHz. In I3C Basic mode, this CCC is ignored. When SETAASA CCC is registered by the SPD5 Hub, it updates MR18 [5] and INF_SEL bit in GETSTATUS CCC = 1 and it takes in effect at the next Start operation (i.e. after STOP operation). Table 79 shows an example of a single SETAASA CCC.

SETAASA CCC does not support PEC function as device is in I^2C mode and there is no PEC function in I^2C mode.

Table 79. SETAASA CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x29 (Broadcast)								T	P

2.7.18.5 GETSTATUS CCC

The GETSTATUS CCC is supported in I3C Basic mode. In I^2C mode, this CCC is ignored (i.e. it is not executed internally and Repeat Start byte arriving after the 0x90 GETSTATUS CCC code is not acknowledged and host must do STOP operation. Table 80 to Table 81 shows an example of a single GETSTATUS CCC.

In I3C Basic mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 80. GETSTATUS CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x90 (Direct)								T	
Sr	DevID[6:0]							R = 1	A[1]	
	PEC_Err	INF_SEL	0	0	0	0	0	0	T	
	0	0	P_Err	0	Pending Interrupt				T	Sr (Note 2) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 81. GETSTATUS CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 3)	
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R = 1	A (Note 3)	
	PEC_Err	INF_SEL	0	0	0	0	0	0	T	
	0	0	P_Err	0	Pending Interrupt				T	
	PEC								T	Sr (Note 4) or P

3. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
4. Repeat Start or Repeat Start with 7'h7E.

Table 82. GETSTATUS CCC Byte Encoding

Bit	Encoding	Notes
PEC_Err	0 = No Error 1 = PEC Error Occurred	This register is cleared when Host issues clear command to MR20 [1] for PEC error.
INF_SEL	0 = I2C Mode 1 = I3C Basic Mode	This register is updated when SETAASA or RSTDAA CCC is registered by the device or when the device goes through bus reset. This register is a copy of MR18 [5].
P_Err	0 = No Error 1 = Protocol Error; Parity error occurred	This register is cleared when Host issues clear command to MR20 [0] for Parity error.
Pending Interrupt	0000 = No Pending Interrupt 0001 = Pending Interrupt All other encodings are reserved	This register is cleared when Host issues clear command to any appropriate device status register that causes IBI status register to get cleared.

When the SPD5 Hub device responds to GETSTATUS CCC, after it completes the response, the PEC_Err, P_Err and Pending Interrupt Bits [3:0] do not automatically get cleared. The host must explicitly clear the appropriate status register through Clear command by writing 1 to corresponding register or by issuing Global Clear command. Once the SPD5 Hub device clears the appropriate status register, only then PEC_Err, P_Err and Pending Interrupt Bits [3:0] gets cleared.

After host issues clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to 1 and Pending Interrupt Bits [3:0] to 0001.

2.7.18.6 DEVCAP CCC

The DEVCAP CCC is only supported after device is put in I3C Basic mode. In I2C mode, it is illegal for host to issue this CCC. Table 83 to Table 84 shows an example of a single DEVCAP CCC.

In I3C Basic mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

Table 83. DEVCAP CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0xE0 (Direct)								T	
Sr	DevID[6:0]							R = 1	A (Note 1)	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	Sr (Note 2) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 84. DEVCAP CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0xE0 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R = 1	A (Note 1)	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	
	PEC								T	Sr (Note 2) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 85. DEVCAP CCC Byte Encoding

Bit	Encoding	Notes
MSB [7]	RFU	Coded as 0
MSB[6]	RFU	Coded as 0
MSB[5]	RFU	Coded as 0
MSB[4]	RFU	Coded as 0
MSB[3]	RFU	Coded as 0
MSB[2]	0 = No Support for Timer based Reset 1 = Supports Timer based Reset	SPD5 Hub hard codes to 1
MSB[1:0]	RFU	Coded as 000
LSB[7:0]	RFU	Coded as 000

2.7.18.7 SETHID CCC

The SPD5118 and SPD5108 supports SETHID CCC. The device behavior is as defined below.

The SETHID CCC is supported only when device is in I^2C mode. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any parity error and to avoid subsequent undesired implication, the host shall limit the maximum speed of operation for this CCC to 4MHz. In I3C Basic mode, it is illegal for host to issue this CCC. When SETHID CCC is registered by the SPD5 Hub, it stops 3-bit HID translation. Table 86 shows an example of a single SETHID CCC. The host must send all 0 in the data byte followed by T bit. The SPD5 Hub device forwards bits [7:4, 0] to local devices behind the SPD5 Hub as it receives from the Host. The SPD5 Hub device substitutes its own 3-bit HID code in bits [3:1] and forwards it to the local devices behind the SPD5 Hub. The SPD5 Hub device also re-calculates the parity information and forwards the updated parity information in T bit. As the device is in I^2C mode when SETHID CCC is issued, the PEC function is not supported.

The Host may issue SETHID CCC more than one time. See Figure 24 and Figure 25 for examples.

Table 86. SETHID CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x61 (Broadcast)								T	
	0	0	0	0	0	0	0	0	T	P

2.7.18.8 DEVCTRL CCC

On a typical I3C Basic bus there can be up to 120 devices. For DDR5 DIMM application environment, there are up to 8 SPD5 Hub devices and behind each SPD5 Hub devices, there are 4 local slave devices totaling up to 40 or more devices on I3C Basic bus. For certain operation such as enable or disable functions that are common to all devices (i.e. Packet Error Check), the host must go through one device at a time which takes significant amount of time at initial power up. Further, it requires additional complexity on the host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I^2C mode or I3C Basic mode of operation. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error and to avoid subsequent undesired implication, the host shall limit the maximum speed of operation for this CCC to 4MHz. Table 87 to Table 88 shows an example of a single DEVCTRL CCC See Figure 24 and Figure 25 for Host flow diagram examples.

In I3C mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

The host must pay attention to DEVCTRL CCC. The DEVCTRL CCC is limited to SPD5 Hub devices volatile register space only and should not be used for SPD5 Hub's NVM operation. If DEVCTRL CCC is used to access device specific registers (e.g. RegMod = 1), the host must still follow any device specific register restriction. For instance, if any device specific register such as IO timing parameter related register require STOP operation for device to take in the effect of the setting, the host must also use STOP operation when using DEVCTRL CCC to access device specific register.

There are additional restrictions that host must pay attention to:

- DEVCTRL CCC must be followed by STOP operation before starting a device specific register access. In other words, host shall avoid DEVCTRL CCC followed by Repeat Start to do a device specific register operation. Note that host is allowed to do multiple DEVCTRL CCC with Repeat Start in between to the same device or across multiple devices.
- DEVCTRL CCC must be followed by STOP operation before starting Default Read Address Pointer Mode even across different devices.
- In I^2C mode, DEVCTRCL CCC must be limited to 1 byte addressing mode for SPD5 Hub device (i.e. MR11 [3] = 0.

Table 87. DEVCTRL CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T (Note 2)	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr (Note 3) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. An exception is made for DEVCTRL CCC where device does report a parity error when it determines the 7-bit device select code issued by the host does not match with its own device code. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 88. DEVCTRL CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T (Note 2)	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC								T	Sr (Note 3) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. An exception is made for DEVCTRL CCC where device does report a parity error when it determines the 7-bit device select code issued by the host does not match with its own device code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity or PEC error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 89. DEVCTRL CCC Command Definition

Parameter	Definition
AddrMask[2:0]	Broadcast, Unicast or Multicast Command Selection 000 = Unicast Command; SPD5 Hub device responds if DevID[6:0] field matches with SPD5 Hub device's own 7-bit address (4-bit LID + 3-bit HID) 011 = Multicast Command; SPD5 Hub device and possible other device responds if DevID[6:3] field matches with SPD5 Hub device's own 4-bit LID address 111 = Broadcast Command; All devices responds to this command All other encodings are reserved
StartOffset[1:0]	Only applicable if RegMod = 0 Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and has continuous access to next byte until STOP operation. If Byte 3 is reached, the host is responsible for applying STOP operation. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC BL[1:0]	Only applicable if RegMod = 0 and PEC function is enabled. Identifies the burst length just for this DEVCTRL CCC. The device uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte
RegMod	Identifies if DEVCTRL is going to be used for General Registers as identified in Byte 0 to Byte 3 or device specific address offset register. 0 = Access to General Registers in Byte 0 to Byte 3 (i.e. StartOffset[1:0] = Valid) 1 = Device Specific Offset Address (i.e. StartOffset[1:0] and PECBL[1:0] is a don't care and does not apply). The Host shall NOT use RegMod = 1 with Broadcast Command if there are different types of devices on the I3C Basic bus.
DevID[6:0]	Identifies 7-bit device address. Device responds to DEVCTRL CCC data packet depending on AddrMask[2:0]. If AddrMask[2:0] = 111, DevID[6:0] is a don't care and device always responds. If AddrMask[2:0] = 000, DevID[6:0] must match for device to respond If AddrMask[2:0] = 011, DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the device always NACKs.

Table 90. DEVCTRL CCC Data Payload Definition

Byte #	Bit #	Function	Definition	Comment
Byte 0	[7]	PEC Enable	0 = Disable 1 = Enable	MR18 [7] is updated
	[6]	Parity Disable	0 = Enable 1 = Disable	MR18 [6] is updated
	[5:2]	RFU	RFU	
	[1]	RSVD	0 = RSVD 1 = RSVD	SPD5 Hub device always ignores this bit.
	[0]	RFU	RFU	
Byte 1	[7:4]	RFU	RFU	
	[3]	Global and IBI Clear	0 = No Action 1 = Clear All Event and pending IBI (Note 1)	MR27 [7] is updated.
	[2:0]	RFU	RFU	
Byte 2	[7:0]	RFU	RFU	
Byte 3	[7:0]	RFU	RFU	

1. After slave device clears the event, the device can still have certain registers set to 1 if the event is still present in which case, the device will generate an IBI again at the next opportunity.

DEVCTRL CCC Examples - RegMod = 0

Table 91 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Multicast command. Host sends Multicast command to all devices with 4-bit LID code of 1001 on I3C Basic bus to do VR Enable followed by all devices with 4-bit LID code of 0110 to disable parity function. The host sends AddrMask = 011 to indicate Multicast command with DevID[6:3] match; StartOffset = 00 to indicate starting Byte 0 and RegMod = 0 to indicates general register. Upon receiving this command, all devices with DevID[6:3] that matches to 1001 will do the VR Enable command and DevID[6:3] that matches to 0110 with disable the parity function.

Table 91. DEVCTRL CCC Example - Multicast Command to 1001 and 0110 Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	1001 000							0	T	
	0000 0010								T	
Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	0110 000							0	T	
	0100 0000								T	P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation.

Table 92 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Broadcast command to enable PEC function. The host sends AddrMask = 111 to indicate Broadcast command; StartOffset = 00 to indicate starting Byte 0 and RegMod = 0 to indicates general register. Upon receiving this command, all devices will enable PEC function.

Table 92. DEVCTRL CCC Example - Broadcast Command to all Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x62 (Broadcast)								T	
	111			00		00		0	T	
	0000 000							0	T	
	1000 0000								T	P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation.

Table 93 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Unitcast command to enable VR on DIMM5. The host sends AddrMask = 000 to indicate Unicast command; StartOffset = 00 to indicate starting Byte 0 and RegMod = 0 to indicates general register. Upon receiving this command, PMIC on DIMM5 will enable its regulator.

Table 93. DEVCTRL CCC Example - Unicast Command to PMIC on DIMM5

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x62 (Broadcast)								T	
	000			00		00		0	T	
	1001 101							0	T	
	0000 0010								T	P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation.

DEVCTRL CCC Examples - RegMod = 1

Table 94 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function enabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of 0010 on the I3C Basic bus to write to address offset of 0x1C and 0x1D with data 0xFF and 0x55, respectively followed by all devices with 4-bit LID of 1001 on the I3C bus to write to address offset of 0x15 with data 0x78.

The PEC calculation starts with Start or Repeat Start operation but does not include 7’h7E with W = 0 byte in PEC calculation.

Table 94. DEVCTRL CCC Example - Multicast Command to 0010 and 1001 Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	0010 000							0	T	
	0001 1100 (address offset 0x1C)								T	
	0010 0000 (CMD field = 2 bytes of data)								T	
	1111 1111 (data)								T	
	0101 0101 (data)								T	
	PEC								T	
Sr	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0101 (address offset 0x15)								T	
	0000 0000 (CMD field = 1 byte of data)								T	
	0111 1000 (data)								T	
	PEC								T	P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation.

Table 95 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of 1001 on the I3C Basic bus to write to address offset of 0x13 with data 0xFF and it continues to write data 0x01 to the next address.

Table 95. DEVCTRL CCC Example - Multicast Command to 1001 Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A (Note 1)	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0011 (address offset 0x13)								T	
	1111 1111 (data)								T	
	0000 0001 (data)								T	P

1. Figure 13 shows how the transition occurs from Slave Open Drain (ACK) to Host Push Pull Operation.

2.7.19 Host Flow Diagram Examples of DDR5 DIMM

Figure 24 and Figure 25 below shows examples of Host flow diagrams when first powers up DDR5 DIMM. The Host may follow any of the flow. The figure includes information for other components (i.e. SPD Hub, RCD, TS) as reference and can be ignored from PMIC design point of view.

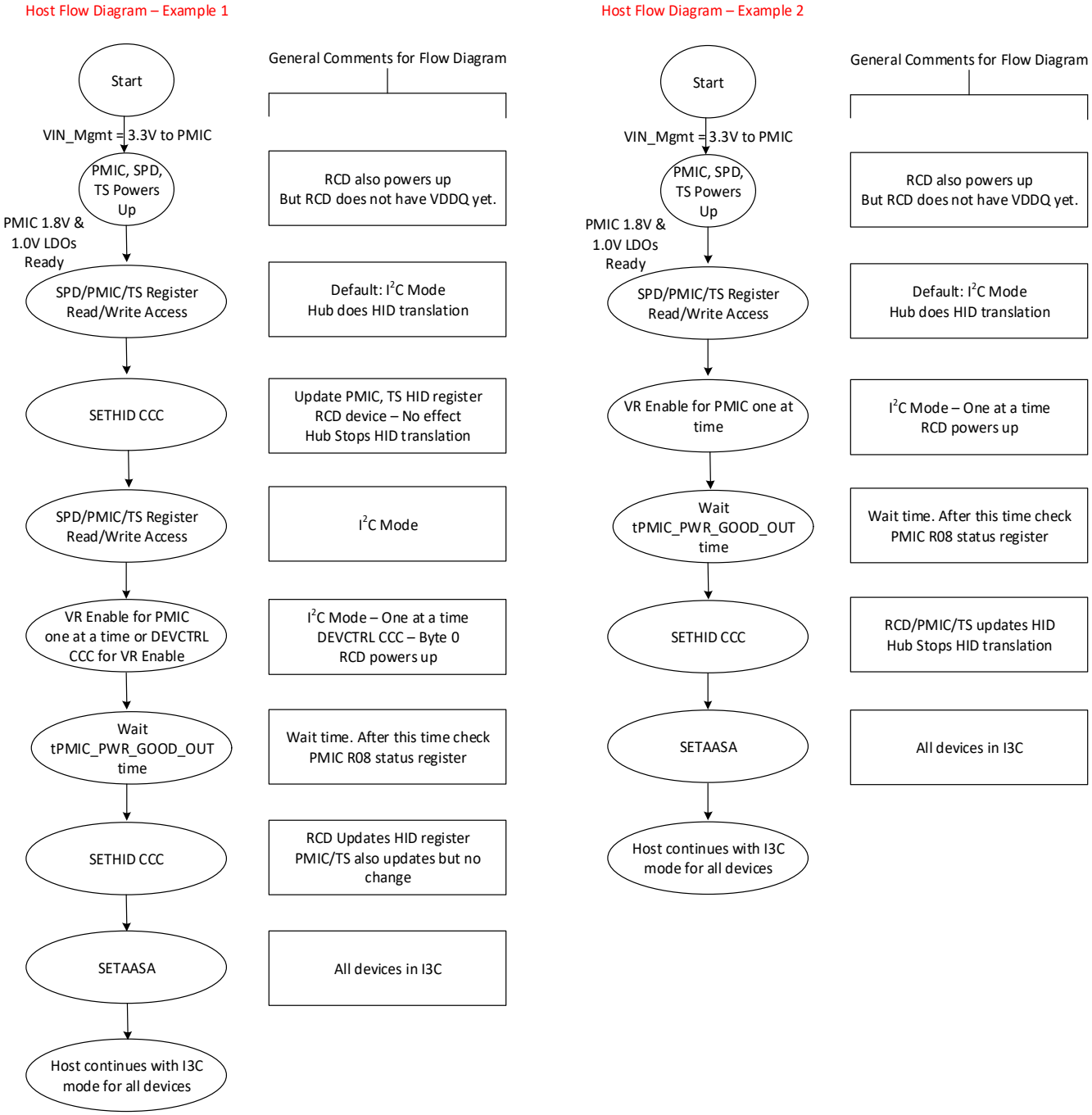


Figure 24. Host Flow Diagram Examples 1 and 2

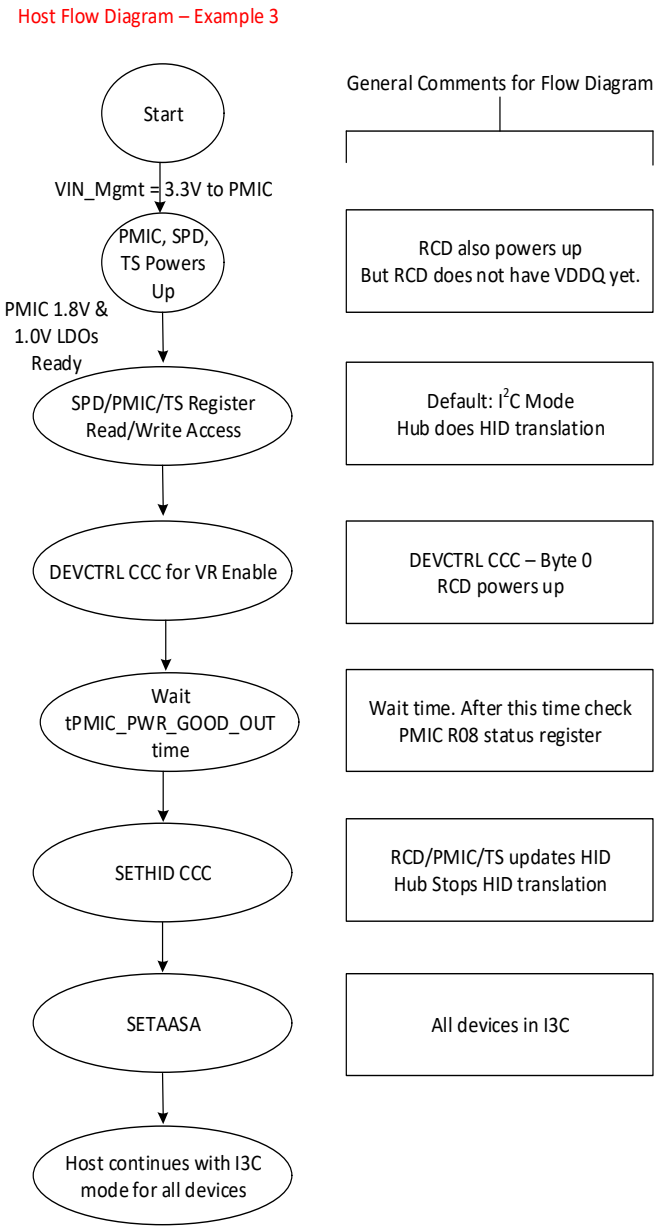


Figure 25. Host Flow Diagram Example 3

2.7.20 IO Operation

The SPD5 Hub device supports configurable IO operation scheme of either Open Drain or Push-Pull on its Host side of the interface (HSCL and HSDA) and Local side of the interface (LSCL and LSDA). Further, the SPD5 Hub device supports independent IO configuration on Host side and Local side of the interface. The voltage levels for either Open Drain mode or Push Pull can also be independently configurable.

At power on, by default, the SPD5 Hub device comes up in I^2C mode of operation with Open Drain IO for both its Host side and Local side of the interface. The maximum speed is limited to 1MHz and supported IO voltage levels are from 1.0V to 3.3V.

After power on, the host may put the SPD5 Hub device in I3C mode of operation. In I3C Basic mode of operation, the maximum speed is limited to 12.5MHz and supported IO voltage levels are from 1.0V to 1.2V or 1.8V.

In I3C Basic mode, the host may drive the HSCL clock input of the SPD5 device using either Push-Pull output driver or using the open-drain output driver. It is expected that for all DDR5 DIMM family environment, the host may always drive the HSCL clock input using a Push-Pull output driver.

To support in band interrupt, the SPD5 device supports dynamic switching between Open Drain mode and Push Pull mode on its HSDA and LSDA bus for various event. The Table 96 describes the different mode of operation by the SPD5 device for each cycle.

Table 96. SPD5 Hub Device Dynamic IO Operation Mode Switching

	SCL, SDA Open Drain Mode	SCL, SDA Push Pull Mode
START + Device Select Code	Yes	No
START + 7'h7E IBI Header Byte	Yes	No
REPEAT START + Device Select Code	No	Yes
REPEAT START + 7'h7E Header Byte	No	Yes
CCC Bytes (i.e. after 7'h7E+W = 0+ACK)	No	Yes
STOP	No	Yes
ACK/NACK Responses	Yes	No
Command, Block Address, Address Operation	No	Yes
Interrupt Request by Slave + Device Select Code	Yes	No
IBI Payload	No	Yes
Write Data, T-bit sequence	No	Yes
Read Data, T-bit sequence	No	Yes
PEC, T-bit sequence	No	Yes

2.7.21 Bus Clear

The SPD Hub device supports the following described Bus Clear feature in I^2C mode only. Any attempt by host to perform I^2C Bus clear on a slave device in I3C mode may result in an active drive bus contention on the SDA data line.

There may be abnormal circumstances when the host abruptly stops clocking SCL while the slave device is in the middle of outputting data for read operation. For these type of events, the SDA data line may appear as stuck low as the device is expecting to receive more clock pulses from the host. Eventually when the host has control of the SCL clock, the host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transaction with Start condition.

2.7.22 Bus Reset

To prevent a malfunctioning device from locking up the I^2C bus or I3C Basic bus, a bus reset mechanism is defined. It uses a timeout mechanism on HSCL as shown in Figure 26 to force a device bus reset. All devices (All SPD5 Hub and all local slave devices behind the hub) on a I^2C or I3C Basic bus reset simultaneously. Bus reset operation works same way regardless of whether device is operating in I^2C or I3C Basic mode.

To guarantee the device resets I^2C bus or I3C Basic bus, the HSCL clock input Low time has to be greater than or equal to $t_{TIMEOUT(Max)}$.

The SPD5 Hub device does not reset I^2C bus or I3C Basic bus if the HSCL clock input Low time is less than $t_{TIMEOUT(Min)}$.

If the HSCL clock input Low time is between $t_{TIMEOUT(Min)}$ and $t_{TIMEOUT(Max)}$, the SPD5 Hub device does not guarantee and it may or may not reset the I^2C bus or I3C Basic bus.

When RESET, the SPD5 Hub device takes following action:

1. Interface and any pending command or transactions are cleared
2. All internal register values are preserved unless noted otherwise in item # 3.

3. Device always returns to I2C mode of operation; MR18 [7:5] = 000; MR27 [4] resets to 0; MR52 [1:0] resets to 00; INF_SEL bit in GETSTATUC CCC to 0.
4. Device does not re-sample HSA pin.
5. Device floats the HSDA pin such that it gets pulled High by the external pull-up. The device pulls the LSDA pin High.
6. Device treats bus reset as STOP operation.

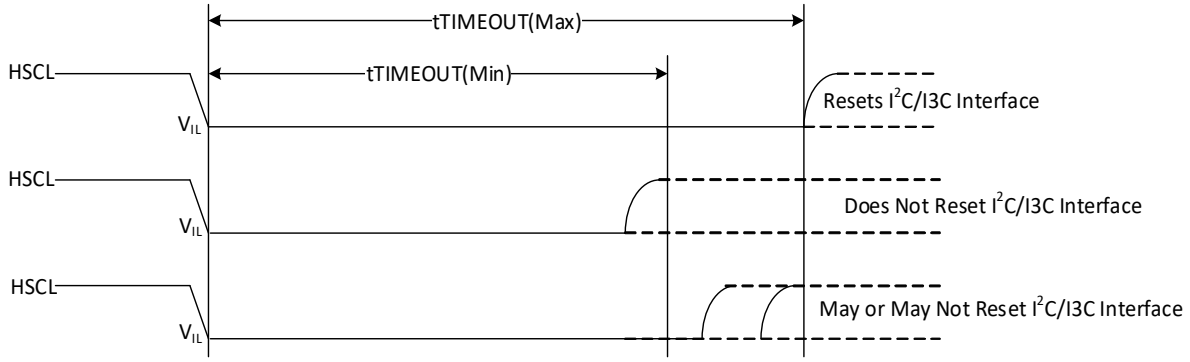


Figure 26. I2C or I3C Basic Bus Reset - SPD5 Hub Device

2.7.23 Command Truth Table

The command truth table as shown in Table 97 only applies in I3C Basic mode with PEC enabled. In I2C mode and I3C Basic mode with PEC disabled, the command truth table does not apply.

Table 97. For I3C Mode Only with PEC Enabled - Command Truth Table

SPD5 Command	Command Name	Command Code	RW	MemReg	Block Address	Address
		2nd Byte Bits [7:5]	2nd Byte Bit [4]	1st Byte Bit [7]	2nd Byte Bits [3:0] 1st Byte Bits [6]	1st Byte Bits [5:0]
Write 1 Byte to Register	W1R	000	0	0	V	V
Read 1 Byte from Register	R1R		1	0	V	V
Write 1 Byte to NVM	W1M		0	1	V	V
Read 1 Byte from NVM	R1M		1	1	V	V
Write 2 Byte to Register	W2R	001	0	0	V	V
Read 2 Byte from Register	R2R		1	0	V	V
Write 2 Byte to NVM	W2M		0	1	V	V
Read 2 Byte from NVM	R2M		1	1	V	V
Write 4 Byte to Register	W4R	010	0	0	V	V
Read 4 Byte from Register	R4R		1	0	V	V
Write 4 Byte to NVM	W4M		0	1	V	V
Read 4 Byte from NVM	R4M		1	1	V	V
Write 16 Byte to Register	W16R	011	0	0	V	V
Read 16 Byte from Register	R16R		1	0	V	V
Write 16 Byte to NVM	W16M		0	1	V	V
Read 16 Byte from NVM	R16M		1	1	V	V
Reserved	RSVD	100 to 111	RSVD	RSVD	RSVD	RSVD

2.8 HSA Pin Resistor Values and ID

2.8.1 SPD5 Family Devices

Table 98 shows the HSA pin resistor values and corresponding ID for the SPD5118 and SPD5108.

Table 98. HSA Pin Resistor Value and ID - SPD5 Family

HSA Pin Connection	SPD ID	Comment
10.0kΩ to GND	HID = 000	1% Resistor
15.4kΩ to GND	HID = 001	
23.2kΩ to GND	HID = 010	
35.7kΩ to GND	HID = 011	
54.9kΩ to GND	HID = 100	
84.5kΩ to GND	HID = 101	
127kΩ to GND	HID = 110	
196kΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline Mode; Write protect override enabled

2.9 SPD5 Family Device - Write and Read Access

In both I^2C and I3C mode, any read or write operation to SPD5 Hub EEPROM memory must be followed by STOP operation (i.e. not Repeat Start) before launching new transactions to SPD5 Hub volatile memory registers. Conversely, any read or write to SPD5 Hub volatile memory registers must be followed by STOP operation (i.e. not Repeat Start) before launching new transactions to SPD5 Hub EEPROM.

2.9.1 Write and Read Access - NVM Memory

For I^2C mode and I3C Basic mode with PEC disabled, the write access to NVM memory is done within 16 byte boundary in a block. Once the last address within 16 byte boundary in a block is reached, the device stops the operation. The write operation to remaining addresses are not executed by the SPD5 Hub device. The SPD5 Hub device does not loop to first address within the 16 byte boundary in that block. The SPD5 Hub device does not set any register to inform this to the host and does not generate any interrupt to the host.

For I3C Basic mode with PEC enabled, if for a given Write access (either W2M, W4M, W16M) to NVM memory reaches the last address within the 16 byte boundary in a block, (i.e. Byte 15, Byte 31, Byte 47, Byte 63), the device stops the operation. The write operation to remaining addresses are not executed by the SPD5 Hub device. The SPD5 Hub device does not loop to first address within the 16 byte boundary in that block. The SPD5 Hub device does not set any register to inform this to the host and does not generate any interrupt to the host.

Unlike Write access to NVM memory, any read access to NVM memory does not impose 16 byte boundary or block boundary. The Read access to NVM memory is treated as continuous address space even if it crosses 16 byte boundary or block boundary in I^2C mode or I3C Basic mode (with or without PEC enabled). The last byte for NVM memory is 1024^{th} byte and when the address pointer reaches to the last byte, the SPD5 Hub device does not return any data. In I^2C mode and I3C Basic mode with PEC disabled, the host must do the STOP operation.

2.9.2 Write and Read Access - Register Memory

There is no concept of “Block Address”. The “Block Address” is treated is simply as upper address bit when MemReg = 0 by the SPD5 Hub device.

For I^2C mode and I3C Basic mode with PEC disabled or PEC enabled, any access to read or write to Register memory is continuous address space even if it appears crossing 16 byte boundary or “Block Address” boundary. The last byte is MR255 and when the address pointer reaches to MR255, the SPD5 Hub device does not return any data. In I^2C mode and I3C Basic mode with PEC disabled, the host must do the STOP operation.

2.10 Write Protection of Non-Volatile Memory (For SPD5 Family Devices Only)

2.10.1 Normal Run Time Operation (HSA Pin is tied to GND via a resistor value)

In this mode, the SPD5 device offers a write protection for its NVM memory. The MR12 [7:0] and MR13 [7:0] register contains a bit map for write protection status of each 64 byte block of NVM memory. The MR12 [7:0] and MR13 [7:0] registers can be written to 1 at any time. When any bit in MR12 or MR13 is set to 1, further writes to that corresponding block of NVM are ignored and MR52 [6] bit is set to 1.

Once any bit is written to 1 in MR12 and MR13, clearing that bit in normal run time mode is not allowed. Any attempt to clear the bit in MR12 and MR13 is ignored and MR52 [5] bit is set to 1.

2.10.2 Offline Tester Operation (HSA Pin is tied directly to GND, no resistor value)

In this mode, the SPD5 device allows to clear any bit in MR12 and MR13 registers. Once cleared, the SPD device allows to modify the corresponding block of NVM memory.

2.10.3 Suggested Steps to Program SPD5 Devices

The recommended steps to program the SPD Hub devices are:

1. Connect HSA Pin directly to GND (without a resistor).
2. Power up the device. The device senses HSA pin. It sets MR48 [2] = 1 and enables write protection override.
3. Program MR12 and MR13 to enable desired NVM blocks to be written.
4. Program desired NVM blocks.
5. Program MR12 and MR13 to set the write protection as desired.

2.11 AC Timing Definition

2.11.1 I2C or I3C Basic Bus Timing

The SPD5 Hub device follow the I2C or I3C Basic bus timing requirements. The Figure 27 and Figure 28 show the timing diagram for Data bus Input and Data Output parameters.

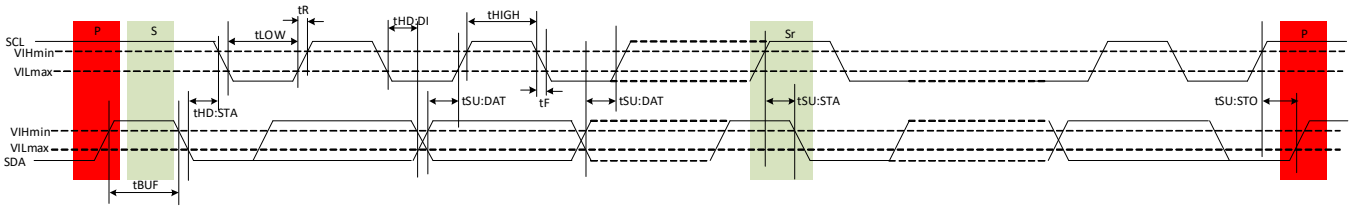


Figure 27. I2C or I3C Basic Bus AC Input Timing Parameter Definition

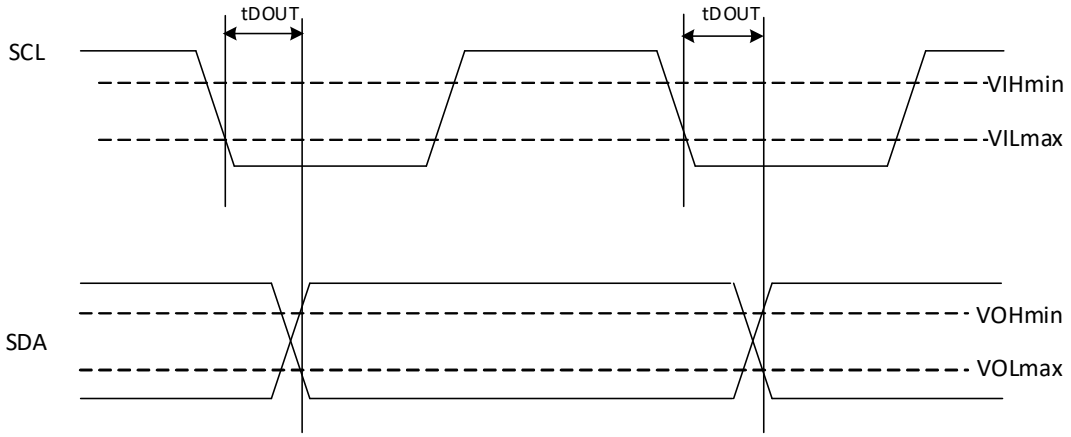


Figure 28. I3C Basic Bus AC Data Output Timing Parameter Definition

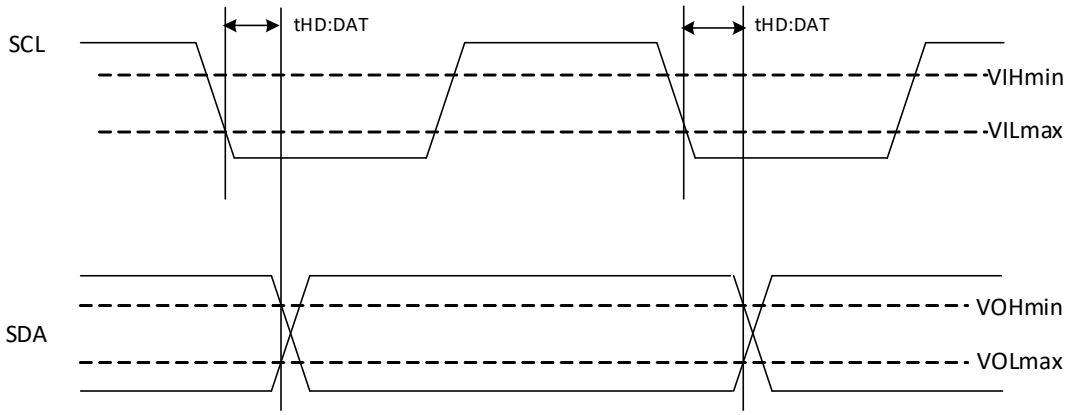


Figure 29. I²C Bus AC Data Output Timing Parameter Definition

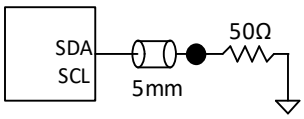


Figure 30. Output Slew Rate and Output Timing Reference Load

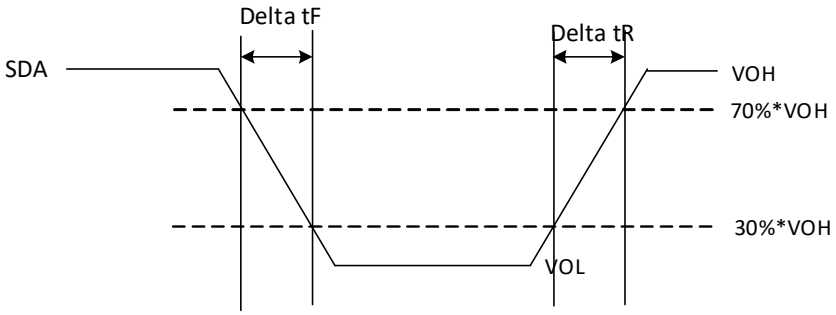


Figure 31. Output Slew Rate Measurement Points

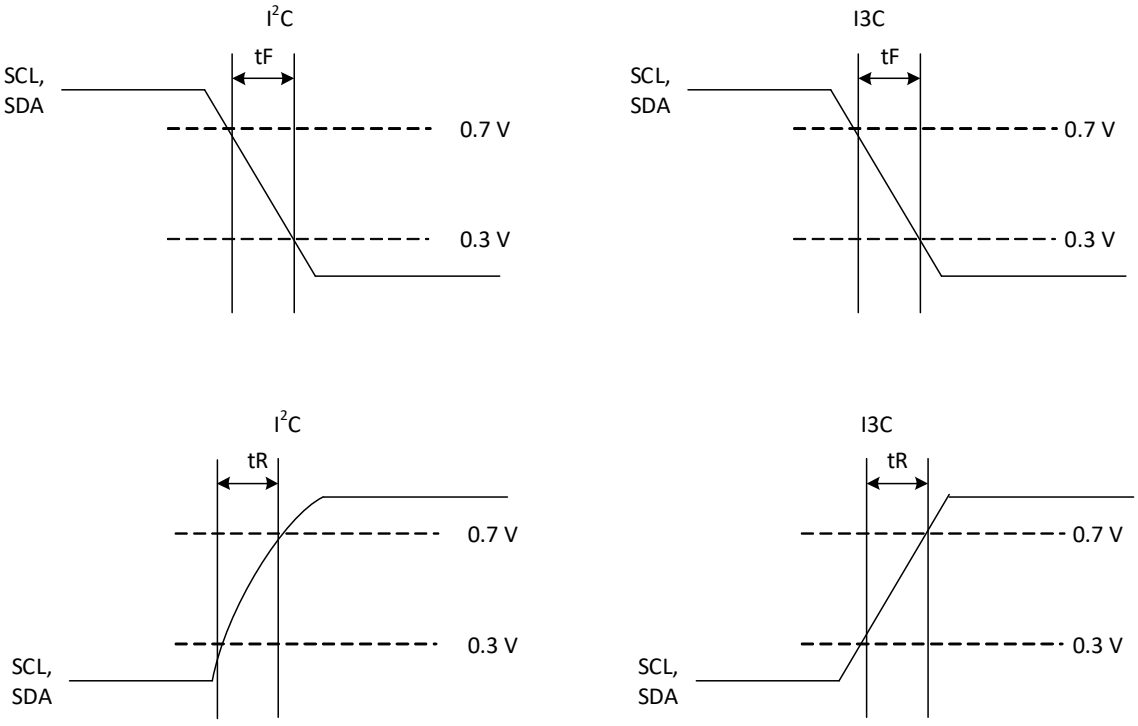


Figure 32. Rise and Fall Timing Parameter Definition

2.11.2 Hub Propagation Delay

The SPD5 Hub device has a propagation delay of tPDHL for its host interface HSCL/HSDA input signals to the local interface LSCL/LSDA signals, respectively.

Similarly, the SPD5 Hub device has a propagation delay of tPDLH for its local interface LSDA input signal to the host interface HSDA signal.

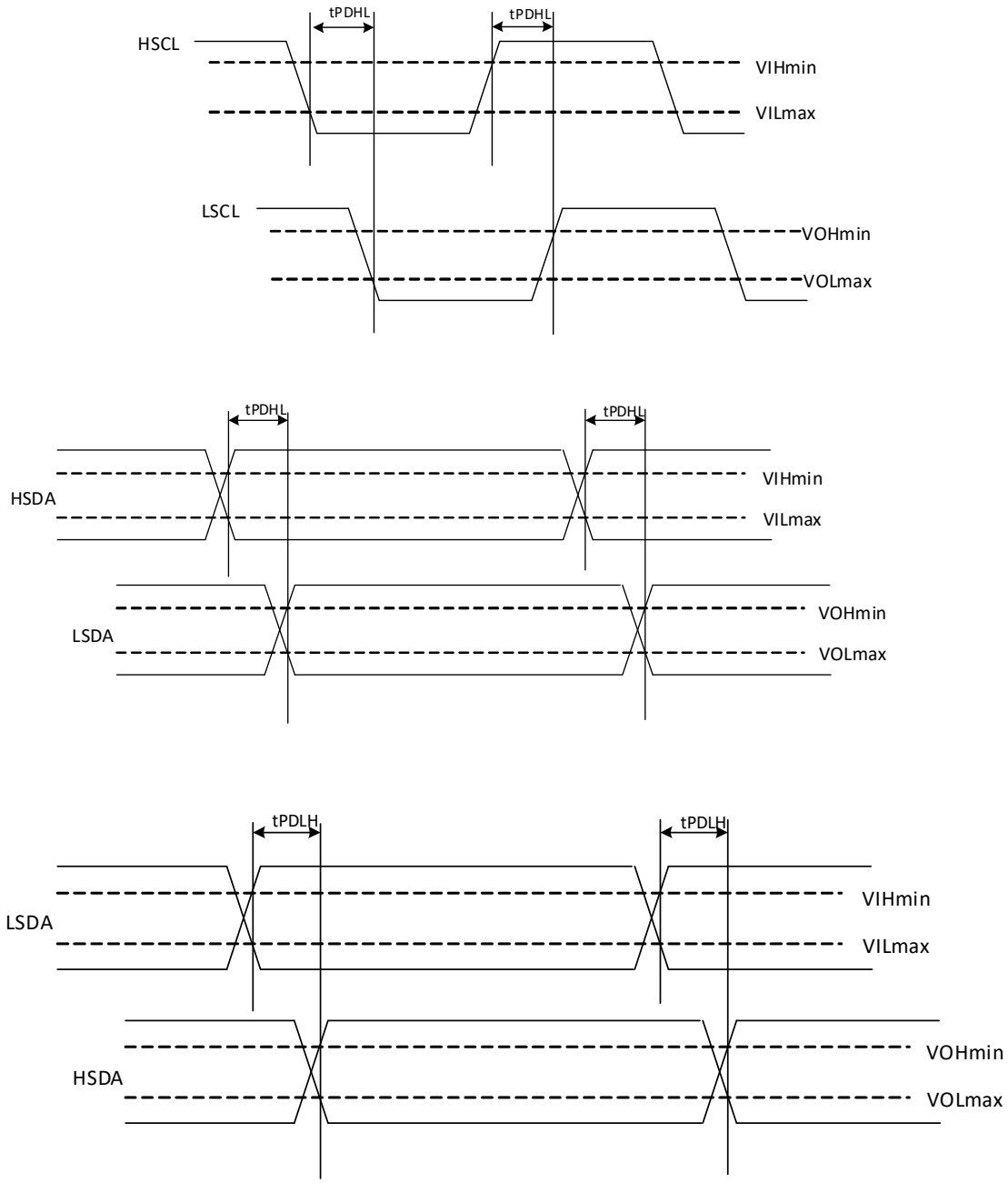


Figure 33. Propagation Delay Through the SPD5 Device

2.12 Parametric Characteristics

2.12.1 Absolute Maximum Ratings

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 99. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
T_{STG}	Storage temperature	-65	150	°C
V_{IO}	Supply voltage	-0.50	2.1	V
V_{DDSPD}	Supply voltage	-0.5	2.1	V
HSA	HSA pin	-0.5	2.1	V
HSCL, HSDA, LSCL, LSDA; I^2C Mode Only	HSCL, HSDA, LSCL, LSDA pins	-0.5	3.6	V
HSCL, HSDA, LSCL, LSDA; I^2C/I3C Basic Mode	HSCL, HSDA, LSCL, LSDA pins	-0.5	2.1	V

2.12.2 ESD Requirements

Table 100. ESD Requirement

Test Model	Pin	Maximum Rating	Sample Size	Unit
HBM	All	±4000	3 lots, 3 ea/lot	V
CDM	All	±500	3 lots, 3 ea/lot	V

2.12.3 Operating Condition, Measurement Condition and DC and AC Characteristics

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables.

Table 101. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DDSPD}	Input Supply Voltage	1.7	1.8	2.0	V
V_{IO}	Input Supply Voltage	0.95	1.0	1.05	V
$V_{LDO\_1.0}$	LDO Output Supply Voltage	0.95	1.0	1.05	V
T_{CASE}	Case Operating Temperature	-40		125	°C
$T_{WRITEOK}$	Case Temperature Range for NVM Write Operation	-40		95	°C

Table 102. Write Endurance and Data Retention

Parameter	Min	Typ	Max	Units
Data Retention (25°C)	TBD	-	-	Years
Write Endurance Cycles at 25°C	100000	-	-	Cycles
Write Endurance Cycles at 95°C	100000	-	-	Cycles

Table 103. AC Measurement Conditions (Note 1)

Symbol	Parameter	Min	Max	Units
C_L	Load capacitance	40		pF
	Input Rise and Fall times - Open Drain	-	50	ns
	Input Rise and Fall times - Push Pull	-	5	ns
	Input Signal Swing Levels	0.2 to 0.8		V
	Input Levels for Timing Reference	0.3 to 0.7		V

1. This AC measurement condition (Table 103 and Table 34) is only for the test purpose in lab.

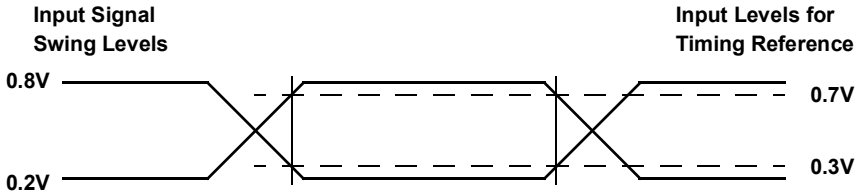


Figure 34. AC Measurement Waveform

Table 104. Input Parameters

Symbol	Parameter (Notes 1, 2)	Test Condition	Min	Max	Units
C_{IN}	Input capacitance (HSDA, HSCL, LSDA)	--	--	5	pF
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	Single glitch, f ≤ 100kHz	--	--	ns
		Single glitch, f > 100kHz	0	50	

1. T_A = 25°C, f = 400kHz.
2. Verified by design and characterization, not necessarily tested on all devices.

Table 105. Output Ron Spec

Symbol	Parameter	Min	Max	Units	Notes
R_{on}	LSCL, LSDA Output Pull-up and Pull-down Driver Impedance	20	100	Ω	1
	HSDA Output Pull-up and Pull-down Driver Impedance	10	40	Ω	1

1. Pull-down R_{on} = Vout/Iout; Pull-up R_{on} = (VIO - Vout)/Iout.

Table 106. DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input leakage current		--	±5	µA
I_{LO}	Output leakage current		--	±5	µA
I_{DDR}	Supply current, read operation	VDDSPD = 1.8V, f_C = 12.5MHz (Note 1)	--	2	mA
I_{DDW}	Supply current, write operation	VDDSPD = 1.8V, f_C = 12.5MHz (Note 1)	--	3	mA
I_{DD1}	Standby Supply current	V_{IN} = VDDSPD = 1.8V	--	TBD	µA
V_{IL}	Input low voltage	--	-0.35	0.3	V
V_{IH}	Input high voltage	--	0.7	3.6	V
V_{OL}	Output low voltage	3mA sink current	--	0.3	V
V_{OH}	Output high voltage	3mA source current	0.75	-	V
I_{OL}	Output low current - HSDA, LSDA, LSCL	V_{OL} = 0.3V		3	mA
I_{OH}	Output high current - HSDA, LSDA, LSCL	V_{OH} = V_{IO} - 0.3V	-3	-	mA

Table 106. DC Characteristics (Continued)

Symbol	Parameter	Test Condition	Min	Max	Unit
Slew_Rate	Rising Output Slew Rate (HSDA, LSDA, LSCL)	(Note 2)	0.1	1.0	V/ns
	Falling Output Slew Rate (HSDA, LSDA, LSCL)		0.1	3.0	V/ns
V_{PON}	Power On Reset threshold	Monotonic rise between V_{PON} and V_{DDSPD}(min) without ringback	1.6	--	V
V_{POFF}	Power Off threshold for warm power on cycle	No ringback above V_{POFF}	--	0.3	V

1. Thermal sensor is active.
2. Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 30 and Figure 31 shows the timing measurement points. For slew rate measurements, the VOH level shown in Figure 31 is a function of R_{on} value; $V_{OH} = \{1.0/(R_{on} + 50)\} * 50$.

Table 107. AC Characteristics

Parameter	Symbol	I²C Mode - Open Drain		I3C Basic Push-Pull (Note 1)		Units	Notes
		Min	Max	Min	Max		
Clock frequency	f_{SCL}	0.01	1	0	12.5	MHz	
Clock pulse width high time	t_{HIGH}	260	--	35	--	ns	
Clock pulse width low time	t_{LOW}	500	--	35	--	ns	
Detect clock low timeout	$t_{TIMEOUT}$	10	35	10	35	ms	
SDA rise time	t_R	--	120	--	5	ns	2, 3
SDA fall time	t_F	--	120	--	5	ns	2, 3
Data in setup time	$t_{SU:DAT}$	50	--	4	--	ns	2
Data in hold time	$t_{HD:DI}$	0		3	--	ns	2
Start condition setup time	$t_{SU:STA}$	260	--	12	--	ns	2
Start condition hold time	$t_{HD:STA}$	260	--	30	--	ns	2
Stop condition setup time	$t_{SU:STO}$	260	--	12	--	ns	2
Time between Stop Condition and next Start Condition	t_{BUF}	500	--	500	--	ns	2, 4
Write time	t_W	--	5		5	ms	
Warm power cycle off time	t_{POFF}	1	--	1	--	ms	
Time from valid 1.8V supply to Sense Valid 1.0V VIO Input	$t_{1.0V\_Ready}$	-	4	-	4	ms	
Time from valid 1.8V supply to Sense HSA pin for HID code assignment	t_{Sense_HSA}	-	5	-	5	ms	
Time from power on to first command	t_{INIT}	10	--	10	--	ms	
Device reinitialization time	t_{RST}			TBD	TBD	ms	
Bus Available time (no edges seen on HSDA and HSCL)	t_{AVAL}			1	--	µs	
Time to issue IBI after an event is detected when Bus is available	t_{IBI_ISSUE}	-	-	-	15	µs	
Time from Clear Register Status to any I3C Basic operation with Start condition to avoid IBI generation; PEC disabled	$t_{CLR\_I3C\_CMD\_Delay}$	-	-	4	-	µs	
Time from Clear Register Status to any I3C Basic operation with Start condition to avoid IBI generation; PEC enabled		-	-	15	-	µs	
Propagation Delay, HSDA to LSDA	t_{PDHL_SPD}		N/A		10	ns	5
Propagation Delay, HSCL to LSCL	t_{PDHL_SPD}		N/A		4.5	ns	5
Propagation Delay, LSDA to HSDA	t_{PDLH_SPD}		N/A		4.5	ns	5
HSCL Falling Clock In to HSDA Data Out Hold Time	$t_{HD:DAT}$	0.5	350	N/A	N/A	ns	6
HSCL Falling Clock In to HSDA Valid Data Out Time	t_{DOUT}	N/A	N/A	0.5	5	ns	7

Table 107. AC Characteristics (Continued)

Parameter	Symbol	I²C Mode - Open Drain		I3C Basic Push-Pull (Note 1)		Units	Notes
		Min	Max	Min	Max		
HSCL Rising Clock In to HSDA Output Off	t_{DOFFS}	N/A	N/A	0.5	12	ns	8
HSCL Rising Clock In to Master HSDA Output Off	t_{DOFFM}	N/A	N/A	0.5	12	ns	9
HSCL Rising Clock In to Master Driving HSDA Signal Low	$t_{CL\_r\_DAT\_f}$	N/A	N/A	40	-	ns	10
DEVCTRL CCC Followed by SPDCTRL CCC or Register Read/Write Command Delay	$t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$	3	-	3	-	µs	11, 12, 13
Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode	$t_{WR\_RD\_DELAY\_PEC\_EN}$	N/A	N/A	8	-	µs	14, 15, 16
SETHID CCC or SETAASA CCC followed by any other CCC or Read/Write Command delay	$t_{I2C\_CCC\_Update\_Delay}$	2.5	-	N/A	N/A	µs	
RSTDAA CCC or ENEC CCC or DISCEC CCC or any other CCC or Read/Write Command Delay	$t_{I3C\_CCC\_Update\_Delay}$	-	-	2.5	-	µs	
Any CCC followed by RSTDAA CCC delay	t_{CCC_Delay}	N/A	N/A	2.5	-	µs	

1. I3C Basic mode with Open Drain operation follows timing values as shown in I²C Mode - Open Drain column.
2. See Figure 27 for input timing parameter definition.
3. See Figure 32 for voltage threshold definition for rise and fall times.
4. If PEC is enabled, $t_{WR\_RD\_DELAY\_PEC\_EN}$ timing parameter also applies.
5. See Figure 30 for output timing parameter measurement reference load definition. See Figure 33 for propagation delay definition.
6. See Figure 29 for output timing parameter definition
7. The Hub device must be configured in I3C Basic mode to guarantee t_{DOUT} value. The input path filter setting is 0 ns. See Figure 28 for output timing parameter definition as well as SCL clock input threshold level and SDA data output threshold level. See Figure 30 for output timing parameter measurement reference load definition.
8. The Hub device must be configured in I3C Basic mode to guarantee t_{DOFFS} value. See Figure 13. See Figure 30 for output timing parameter measurement reference load definition.
9. The Hub device must be configured in I3C Basic mode. The Host guarantees t_{DOFFM} value. See Figure 14. See Figure 30 for output timing parameter measurement reference load definition.
10. See Figure 16.
11. From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay.
12. The device sends NACK if Host does not satisfy $t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$ timing parameter.
13. This timing parameter restriction is only applicable when PEC function is disabled in SPD5 Hub. If PEC is enabled, this timing parameter does not apply.
14. From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay.
15. This timing parameter restriction is only applicable when PEC function is enabled in SPD5 Hub. If PEC is disabled, this timing parameter does not apply.
16. The SPD5 Hub sends NACK if Host does not satisfy $t_{WR\_RD\_DELAY\_PEC\_EN}$ timing parameter.

2.12.4 Temperature Sensor Performance

Table 108. Temperature Sensor Performance,

Parameter	Test Conditions	Min	Typ	Max	Unit
Temperature Sensor Accuracy (Active Range)	$75°C \le T_A \le 95°C$	--	±0.5	±1.0	°C
Temperature Sensor Accuracy (Monitor Range)	$40°C \le T_A \le 125°C$	--	±1.0	±2.0	°C
Temperature Sensor Accuracy (Industrial Temperature Range)	$-40°C \le T_A \le 125°C$	--	±2.0	±3.0	°C
Resolution			0.25		°C
Conversion Time	Assumes 0.25°C accuracy			68	ms
Hysteresis between Temperature Events		1	-	-	°C

3. Volatile Registers Space

3.1 Access Mechanism

3.1.1 Register Attribute Definition

All volatile registers have Base Attributes as defined in Table 109. Some register attributes are further modified with Attribute Modifiers, as defined in Table 110.

The volatile register space has a continuous address. Unlike Non-Volatile memory in SPD5 device, there is no concept of “Block” memory in volatile register space. When writing to and reading from volatile register space (i.e. MemReg = 0), the “Block Address bits” are treated simply as Upper address bits.

Table 109. Register Base Attributes

Attribute	Abbreviation	Description
Read Only	R	This bit can be read by software. Writes have no effect.
Read/Write	RW	This bit can be read or written by software.
Write Only	W	This bit can only be written by software.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by software. The bit will return 0 when read. When writing this bit, software must preserve the value read unless otherwise indicated.

Table 110. Register Attribute Modifier

Attribute	Abbreviation	Description
Write 1 Only	1O	This bit can only be set (i.e. write 1) but not reset (i.e. write 0)
Protected	P	This bit is protected by the password registers TBD. This bit cannot be written to unless the password code has been written into the password registers.
Persistent	E	Persistent.

3.2 Registers

3.2.1 Register Map

Table 111. Register Map

Register Name	Register Address (hex)	Attribute	Description
MR0	0x00	ROE	Device Type; Most Significant Byte
MR1	0x01	ROE	Device Type; Least Significant Byte
MR2	0x02	ROE	Device Revision
MR3	0x03	ROE	Vendor ID Byte 0
MR4	0x04	ROE	Vendor ID Byte 1
MR5	0x05	ROE	Device Capability
MR6	0x06	ROE	Device Write Recovery Time Capability
MR7 to MR10	0x07 to 0x0A	RV	Reserved
MR11	0x0B	RW	I^2C Legacy Mode Device Configuration
MR12	0x0C	RWE	Write Protection For NVM Blocks [7:0]
MR13	0x0D	RWE	Write Protection for NVM Blocks [15:8]
MR14	0x0E	RWE	Device Configuration - Host and Local Interface IO
MR15	0x0F	RWE	Device Configuration - Local Interface Pull-up Resistors
MR16 to MR17	0x10 to 0x11	RV	Reserved

Table 111. Register Map

Register Name	Register Address (hex)	Attribute	Description
MR18	0x12	RO, RW	Device Configuration
MR19	0x13	1O	Clear Register MR51 Temperature Status Command
MR20	0x14	1O	Clear Register MR52 Error Status Command
MR21 to MR25	0x15 to 0x19	RV	Reserved
MR26	0x1A	RW	TS Configuration
MR27	0x1B	RO, RW	Interrupt Configurations
MR28	0x1C	RW	TS Temp High Limit Configuration - Low Byte
MR29	0x1D	RW	TS Temp High Limit Configuration - High Byte
MR30	0x1E	RW	TS Temp Low Limit Configuration - Low Byte
MR31	0x1F	RW	TS Temp Low Limit Configuration - High Byte
MR32	0x20	RW	TS Critical Temp High Limit Configuration - Low Byte
MR33	0x21	RW	TS Critical Temp High Limit Configuration - High Byte
MR34	0x22	RW	TS Critical Temp Low Limit Configuration - Low Byte
MR35	0x23	RW	TS Critical Temp Low Limit Configuration - High Byte
MR36 to MR47	0x24 to 0x2F	RV	Reserved for Device Configuration Type of Registers
MR48	0x30	RO	Device Status
MR49	0x31	RO	TS Current Sensed Temperature - Low Byte
MR50	0x32	RO	TS Current Sensed Temperature - High Byte
MR51	0x33	RO	TS Temperature Status
MR52	0x34	RO	Hub, Thermal and NVM Error Status
MR53 to MR63	0x35 to 0x3F	RV	Reserved

3.2.2 Thermal Sensor Registers Read Out Mechanism

All thermal registers are sixteen bit quantities stored in two consecutive registers; low byte first and then high byte. Five bits are reserved for future use. Reserved bits are Read Only bits and must be set to 0 when Host write the low byte and high byte. The device always returns 0 in Reserved bits when Host reads from the low and high byte. Remaining eleven bits in these paired register form a signed value of multiples of 0.25 ranging from -256.00 to + 255.75. Units for all thermal registers are ºC.

The format of each pair of thermal registers is shown in Table 112.

Table 112. Thermal Register - Low Byte and High Byte

Register		7	6	5	4	3	2	1	0
MRX	Low Byte	8	4	2	1	0.5	0.25	RSVD	RSVD
MRX + 1	High Byte	RSVD	RSVD	RSVD	Sign	128	64	32	16

The examples (reserved bits in grey, sign bit highlighted in cyan) is shown in Table 113.

Table 113. Thermal Register Examples

High Byte	Low Byte	Value	Unit
000 0 0101	1111 00 00	+95.00	ºC
000 0 0101	0101 00 00	+ 85.00	ºC
000 0 0100	1011 00 00	+ 75.00	ºC
000 0 0000	0001 00 00	+ 1.00	ºC

Table 113. Thermal Register Examples (Continued)

High Byte	Low Byte	Value	Unit
000 0 0000	0000 11 00	+ 0.75	°C
000 0 0000	0000 10 00	+ 0.50	°C
000 0 0000	0000 01 00	+ 0.25	°C
000 0 0000	0000 00 00	0.00	°C
000 1 1111	1111 11 00	-0.25	°C
000 1 1111	1111 10 00	-0.50	°C
000 1 1111	1111 01 00	-0.75	°C
000 1 1111	1111 00 00	-1.00	°C
000 1 1101	1000 00 00	-40.00	°C

3.2.3 Register Description

Table 114. MR0

Addr	MR0		Device Type; Most Significant Byte (Note 1)
Bits	Attr	Default	Description
7:0	ROE	-	MR0[7:0]: MSB_DEV_TYPE Device Type - These are hard coded. Once programmed by Renesas, it cannot be changed. 0x51: SPD Device; with Hub Function 0x52; SPD Device; without Hub Function

1. The code in this register is used in conjunction with any device type in MR1 register.

Table 115. MR1

Addr	MR1		Device Type; Least Significant Byte (Note 1)
Bits	Attr	Default	Description
7:0	ROE	-	MR1[7:0]: LSB_DEV_TYPE Device Type - Temp Sensor - These are hard coded. Once programmed by Renesas, it cannot be changed. 0x18: with Temp Sensor; SPD Device 0x08: without Temp Sensor; SPD Device

1. The code in this register is used in conjunction with any device type in MR0 register.

Table 116. MR2

Addr	MR2		Device Revision
Bits	Attr	Default	Description
7:6	RV	0	MR2[7:6]: Reserved
5:4	ROE	01	MR2[5:4]: DEV_REV_MAJOR Major Revision 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
3:1	ROE	001	MR2[3:1]: DEV_REV_MINOR Minor Revision 000 = Revision 0 001 = Revision 1 010 = Revision 2 ... 111 = Revision 7
0	RV	0	MR2[0]: Reserved

Table 117. MR3

Addr	MR3		Device Revision
Bits	Attr	Default	Description
7:0	ROE	0x80	MR3[7:0]: VENDOR_ID_BYTE0 Vendor ID Byte 0 The JEDEC standard Renesas Code.

Table 118. MR4

Addr	MR4		Device Revision
Bits	Attr	Default	Description
7:0	ROE	0xB3	MR4[7:0]: VENDOR_ID_BYTE1 Vendor ID Byte 1 The JEDEC standard Renesas Code.

Table 119. MR5

Addr	MR5		Device Capability
Bits	Attr	Default	Description
7:2	RV	0	MR5[7:2]: Reserved
1	ROE	-	MR6[1]: TS_SUPPORT Internal Temp Sensor Support 0 = Does not support Temp Sensor 1 = Supports Temp Sensor
0	ROE	-	MR6[0]: HUB_SUPPORT Hub Function Support 0 = Does not support Hub function 1 = Supports Hub function

Table 120. MR6

Addr	MR6		Write Recovery Time
Bits	Attr	Default	Description
7:4	ROE	0101	MR6[7:4]: WR_REC_UNIT Write Recovery Unit 0000 = 0 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 50 1100 = 100 1101 = 200 1110 = 500 1111 = Reserved
3:2	RV	0	MR6[3:2]: Reserved
1:0	ROE	10	MR6[1:0]: WR_REC_UNIT_TIME Write Recovery Time Unit 00 = ns 01 = µs 10 = ms 11 = Reserved

Table 121. MR11

Addr	MR11	Default	I²C Legacy Mode Device Configuration
Bits	Attr		Description
7:4	RV	0	MR11[7:4]: Reserved
3	RW	0	MR11[3]: I²C_LEGACY_MODE_ADDR SPD5 Device - I²C Legacy Mode Addressing 0 = 1 Byte Addressing for SPD5 Device Memory 1 = 2 Bytes Addressing for SPD5 Device Memory
2:0	RW	000	MR11[2:0]: I²C_LEGAACY_MODE_ADDR_POINTER SPD5 Device - Non Volatile Memory Address Page Pointer in I²C Legacy Mode (Notes 1, 2, 3) 000 = Page 0 (0x00 to 0x7F) 001 = Page 1 (0x80 to 0xFF) 010 = Page 2 (0x100 to 0x17F) 011 = Page 3 (0x180 to 0x1FF) 100 = Page 4 (0x200 to 0x27F) 101 = Page 5 (0x280 to 0x2FF) 110 = Page 6 (0x300 to 0x37F) 111 = Page 7 (0x380 to 0x3FF)

1. This register is only applicable if bit [3] = 0 and MR18 [5] = 0. The SPD5 Hub device does not incur any delay to switch from one page to another page.
2. This register only applies to non-volatile memory (1024 Bytes) access of SPD5 Hub device. For volatile memory access, this register must be programmed to 000.
3. See Write and Read Access - NVM Memory for the NVM Write and Read operation when device reaches the last byte of the 16 byte block boundary.

Table 122. MR12

Addr	MR12	Default	NVM Protection Configuration For Blocks [7:0] (Notes 1, 2)
Bits	Attr		Description
7	RWE	0	MR12[7]: WP_BLK_7 Write Protect - Block 7 0 = Not Protected 1 = Protected
6	RWE	0	MR12[6]: WP_BLK_6 Write Protect - Block 6 0 = Not Protected 1 = Protected
5	RWE	0	MR12[5]: WP_BLK_5 Write Protect - Block 5 0 = Not Protected 1 = Protected
4	RWE	0	MR12[4]: WP_BLK_4 Write Protect - Block 4 0 = Not Protected 1 = Protected
3	RWE	0	MR12[3]: WP_BLK_3 Write Protect - Block 3 0 = Not Protected 1 = Protected
2	RWE	0	MR12[2]: WP_BLK_2 Write Protect - Block 2 0 = Not Protected 1 = Protected
1	RWE	0	MR12[1]: WP_BLK_1 Write Protect - Block 1 0 = Not Protected 1 = Protected

Table 122. MR12 (Continued)

Addr	MR12		NVM Protection Configuration For Blocks [7:0] (Notes 1, 2)
Bits	Attr	Default	Description
0	RWE	0	MR12[0]: WP_BLK_0 Write Protect - Block 0 0 = Not Protected 1 = Protected

1. Once any register bit is set to 1, it can only be cleared when the SPD5 device is in offline tester mode of operation.
2. The write (or update) transaction to this register must be followed by STOP operation to allow the SPD Hub device to update the setting.

Table 123. MR13

Addr	MR13		NVM Protection Configuration For Blocks [15:8] (Notes 1, 2)
Bits	Attr	Default	Description
7	RWE	0	MR13[7]: WP_BLK_15 Write Protect - Block 15 0 = Not Protected 1 = Protected
6	RWE	0	MR13[6]: WP_BLK_14 Write Protect - Block 14 0 = Not Protected 1 = Protected
5	RWE	0	MR13[5]: WP_BLK_13 Write Protect - Block 13 0 = Not Protected 1 = Protected
4	RWE	0	MR13[4]: WP_BLK_12 Write Protect - Block 12 0 = Not Protected 1 = Protected
3	RWE	0	MR13[3]: WP_BLK_11 Write Protect - Block 11 0 = Not Protected 1 = Protected
2	RWE	0	MR13[2]: WP_BLK_10 Write Protect - Block 10 0 = Not Protected 1 = Protected
1	RWE	0	MR13[1]: WP_BLK_9 Write Protect - Block 9 0 = Not Protected 1 = Protected
0	RWE	0	MR13[0]: WP_BLK_8 Write Protect - Block 8 0 = Not Protected 1 = Protected

1. Once any register bit is set to 1, it can only be cleared when the SPD5 device is in offline tester mode of operation.
2. The write (or update) transaction to this register must be followed by STOP operation to allow the SPD Hub device to update the setting.

Table 124. MR14

Addr	MR14		Device Configuration- Local Interface (Notes 1, 2)
Bits	Attr	Default	Description
7:6	RV	0	MR14[7:6]: Reserved
5	RWE	0	MR14[5]: LOCAL_INF_PULLUP_CONF Local Interface - Pull-up Resistor Configuration 0 = Internal (on die) Pull-up Resistor (Notes 3, 4) 1 = External (board) Pull-up Resistor (Note 5)

Table 124. MR14

Addr	MR14		Device Configuration- Local Interface (Notes 1, 2)
Bits	Attr	Default	Description
4:2	RWE	000	MR14[4:2]: LOCAL_INF_IO_LEVEL Local Interface - IO Voltage Level (Note 6) 000 = 1.0V 001 = 1.1V 010 = 1.2V 011 = 1.8V 100 = 2.5V 101 = 3.3V 110 = Reserved 111 = Reserved
1:0	RV	0	MR14[1:0]: Reserved

1. DIMM Vendor configures this register during assembly based on the DIMM design. After SPD Hub device is powered up, the Host can alter the setting through this register.
2. The write (or update) transaction to this register must be followed by STOP operation to allow the SPD Hub device to update the setting.
3. The pull-up resistor value is configured in MR15 [7:0] for relevant output.
4. The register setting in MR14 [4:2] must be either 000 or 001 or 010 or 011. The internal LDO of the device regulates to either 1.0V or 1.1V or 1.2V depending on the register setting of MR14 [4:2]. If MR14 [4:2] is set to 1.8V (i.e. 011), the device simply connects VDDSPD supply input to the VIO pin internally on die.
5. External pull-up resistor on board to the rail is configured appropriately in register MR14 [4:2]. The device allows any combination of setting in MR14 [4:2] register.
6. This register is configured by the DIMM vendor for the local interface. But it may also be used by the SPD5 Hub device internally for the Host side of the interface.

Table 125. MR15

Addr	MR15		Local Interface - Pull-up Resistor Configuration (Notes 1, 2, 3)
Bits	Attr	Default	Description
7:4	RV	0	MR15[7:4]: Reserved.
3:2	RWE	01	MR15[3:2]: LSDA_PU_RES LSDA or LSDA Pull-up Resistor Select (Note 4) 00 = 0.5kΩ 01 = 1kΩ 10 = 2kΩ 11 = 4kΩ
1:0	RWE	01	MR15[1:0]: LSCL_PU_RES LSCL or LSCL Pull-up Resistor Select (Note 4) 00 = 0.5kΩ 01 = 1kΩ 10 = 2kΩ 11 = 4kΩ

1. This register is only applicable if MR14 [5] = 0.
2. DIMM Vendor can configure this register during assembly based on the DIMM design. After SPD5 Hub device is powered up, the Host can alter the setting through this register.
3. The write (or update) transaction to this register must be followed by STOP operation to allow the SPD Hub device to update the setting.
4. The resistor tolerance is ± 25%

Table 126. MR18

Addr	MR18		Device Configuration (Note 1)
Bits	Attr	Default	Description
7	RW	0	MR18[7]: PEC_EN PEC Enable (Notes 2, 3) 0 = Disable 1 = Enable

Table 126. MR18

Addr	MR18		Device Configuration (Note 1)
Bits	Attr	Default	Description
6	RW	0	MR18[6]: PAR_DIS Parity (T bit) Disable (Notes 3, 4) 0 = Enable 1 = Disable
5	RO	0	MR18[5]: INF_SEL Interface Selection 0 = I^2C Protocol (Max speed of 1MHz) 1 = I3C Protocol (Note 5)
4	RW	0	MR18[4]: DEF_RD_ADDR_POINT_EN Default Read Address Pointer Enable 0 = Disable Default Read Address Pointer (Address pointer is set by the Host) (Note 6) 1 = Enable Default Read Address Pointer; Address selected by register bits [3:2]
3:2	RW	0	MR18[3:2]: DEF_RD_ADDR_POINT_START Default Read Pointer Starting Address (Note 7) 00 = MR49 01 = Reserved 10 = Reserved 11 = Reserved
1	RW	0	MR18[1]: DEF_RD_ADDR_POINT_BL Burst Length for Read Pointer Address for PEC Calculation (Note 8) 0 = 2 Bytes 1 = 4 Bytes
0	RV	0	MR18[0]: Reserved

1. The write (or update) transaction to this register must be followed by STOP operation to allow the SPD Hub device to update the setting.
2. This register is only applicable if MR18 [5] = 1.
3. This register is updated when RSTDAA CCC is registered by the SPD5 Hub device or when SPD5 Hub device goes through the bus reset as described in Bus Reset.
4. This register is only applicable if MR18 [5] = 1. When Parity function is disabled, the SPD5 Hub device simply ignores the T bit information from the Host. The host may actually choose to compute the parity and send that information in T bit or simply drive static low or high in T bit.
5. This register is automatically updated when SETAASA CCC or RSTDAA CCC is registered by the SPD5 Hub device or when SPD5 Hub device goes through bus reset as described in Bus Reset. This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I^2C mode or I3C mode of operation. When this register is updated, it takes effect when there is a next START operation (i.e. after STOP operation).
6. The setting in registerMR18 [3:1] is a don't care.
7. This register is only applicable if MR18 [4] = 1.
8. This register is only applicable if MR18 [7, 4] = 11.

Table 127. MR19

Addr	MR19	Default	Clear Register Command (Note 1)
Bits	Attr		Description
7:4	RV	0	MR19[7:4]: Reserved
3	1O	0	MR19 [3]: CLR_TS_CRIT_LOW Clear Temp Sensor Critical Low Status 1 = Clear MR51 [3] Register
2	1O	0	MR19 [2]: CLR_TS_CRIT_HIGH Clear Temp Sensor Critical High Status 1 = Clear MR51 [2] Register
1	1O	0	MR19 [1]: CLR_TS_LOW Clear Temp Sensor Low Status 1 = Clear MR51 [1] Register
0	1O	0	MR19 [0]: CLR_TS_HIGH Clear Temp Sensor High Status 1 = Clear MR51 [0] Register

1. This entire register is self clearing register after corresponding register is cleared.

Table 128. MR20

Addr	MR20	Default	Clear Register Command (Note 1)
Bits	Attr		Description
7	1O	0	MR20[7]: CLR_SPD_BUSY_ERROR Clear Write or Read Attempt while SPD Device Busy Error Status 1 = Clear MR52 [7] Register
6	1O	0	MR20[6]: CLR_WR_NVM_BLK_ERROR Clear Write Attempt to Protected NVM Block Error Status 1 = Clear MR52 [6] Register
5	1O	0	MR20[5]: CLR_WR_NVM_PRO_REG_ERROR Clear Write Attempt to NVM Protection Register Error Status 1 = Clear MR52 [5] Register
4:2	RV	0	MR20[4:2]: Reserved
1	1O	0	MR20[1]: CLR_PEC_ERROR Clear Packet Error Status 1 = Clear MR52 [1] Register
0	1O	0	MR20[0]: CLR_PAR_ERROR Clear Parity Error Status 1 = Clear MR52 [0] Register

1. This entire register is self clearing register after corresponding register is cleared.

Table 129. MR26

Addr	MR26	Default	Thermal Sensor Configuration (Note 1)
Bits	Attr		Description
7:1	RV	0	MR26[7:1] Reserved
0	RW	0	MR26[0]: DIS_TS Disable Temp Sensor (Note 2) 0 = Enable thermal sensor 1 = Disable thermal sensor

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. If this bit is set to 1 and then reset to 0, the host must wait minimum of tINIT before accessing samples on the thermal sensor.

Table 130. MR27

Addr	MR27	Default	Interrupt Configuration
Bits	Attr		Description
7	1O	0	MR27[7]: CLR_GLOBAL Global Clear Event Status and In Band Interrupt Status (Notes 1, 2) 1 = Clear MR48 [7], MR51 [3:0] and MR52 [7:5,3,1:0] Register
6:5	RV	0	MR27[6:5]: Reserved
4	RO	0	MR27 [4]: IBI_ERROR_EN In Band Error Interrupt Enable for MR52 Error Log (Note 3) 0 = Disable; Errors logged in MR52[7:5, 1:0] registers do not generate an IBI to Host 1 = Enable; Errors logged in MR52 [7:5, 1:0] registers generates an IBI to Host
3	RW	0	MR27 [3]: IBI_TS_CRIT_LOW_EN In Band Error Interrupt Enable for Temp Sensor Critical Low (Note 4) 0 = Disable; MR51[3] = 1 does not generate an IBI to Host 1 = Enable; MR51[3] = 1 and MR27 [4] = 1 generates an IBI to Host
2	RW	0	MR27[2]: IBI_TS_CRIT_HIGH_EN In Band Error Interrupt Enable for Temp Sensor Critical High (Note 4) 0 = Disable; MR51[2] = 1 does not generate an IBI to Host 1 = Enable; MR51[2] = 1 and MR27 [4] = 1 generates an IBI to Host
1	RW	0	MR27[1]: IBI_TS_LOW_EN In Band Error Interrupt Enable for Temp Sensor Low (Note 4) 0 = Disable; MR51[1] = 1 does not generate an IBI to Host 1 = Enable; MR51[1] = 1 and MR27 [4] = 1 generates an IBI to Host
0	RW	0	MR27[0]: IBI_TS_HIGH_EN (Note 4) 0 = Disable; MR51[0] = 1 does not generate an IBI to Host 1 = Enable; MR51[0] = 1 and MR27 [4] = 1 generates an IBI to Host

1. This register is a self clearing register after corresponding registers are cleared. Writing 0 in this register has no effect.
2. After this command is issued, the device does not generate an IBI for any pending event. But if new event occurs, the device does generate an IBI.
3. This register is automatically updated when ENEC CCC or DISEC CCC or RSTDAA CCC is registered by the SPD5 Hub device or when SPD5 Hub device goes through bus reset as described in Bus Reset. This register can be read by the Host through normal read operation but cannot be written with normal write operation either in I^2C mode or I3C mode. When this register is updated, it takes effect when there is a next START operation (i.e. after STOP operation).
4. This register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.

Table 131. MR28

Addr	MR28	Default	Thermal Sensor High Limit Configuration - Low Byte (Notes 1, 2, 3)
Bits	Attr		Description
7:0	RW	0x70	MR28[7:0]: TS_HIGH_LIMIT_LOW MR28 and MR29 - 16 bit thermal registers define the high limit for thermal sensor. See Table 112.

1. This entire register is only applicable ifMR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR28 [7:0] and MR29 [7:0].
3. The Reserved bits are Read Only bits. The Host must write 0 in reserved bits when writing and device always returns 0 when host reads this byte.

Table 132. MR29

Addr	MR29		Thermal Sensor High Limit Configuration - High Byte (Notes 1, 2, 3)
Bits	Attr	Default	Description
7:0	RW	0x03	MR29[7:0]: TS_HIGH_LIMIT_HIGH MR28 and MR29 - 16 bit thermal registers define the high limit for thermal sensor. See Table 112.

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR28 [7:0] and MR29 [7:0].
3. The Reserved bits are Read Only bits. The Host must write 0 in reserved bits when writing and device always returns 0 when host reads this byte.

Table 133. MR30

Addr	MR30		Thermal Sensor Low Limit Configuration - Low Byte (Notes 1, 2, 3)
Bits	Attr	Default	Description
7:0	RW	0	MR30[7:0]: TS_LOW_LIMIT_LOW MR30 and MR31 - 16 bit thermal registers define the low limit for thermal sensor. See Table 112

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. Critical temperature Low Limit value must have a lower value than temperature Low Limit (MR30 [7:0] and MR31 [7:0]
3. The Reserved bits are Read Only bits. The Host must write 0 in reserved bits when writing and device always returns 0 when host reads this byte.

Table 134. MR31

Addr	MR31		Thermal Sensor Low Limit Configuration - High Byte (Notes 1, 2, 3)
Bits	Attr	Default	Description
7:0	RW	0	MR31[7:0]: TS_LOW_LIMIT_HIGH MR30 and MR31 - 16 bit thermal registers define the low limit for thermal sensor. See Table 112

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. Critical temperature Low Limit value must have a lower value than temperature Low Limit (MR30 [7:0] and MR31 [7:0].
3. The Reserved bits are Read Only bits. The Host must write 0 in reserved bits when writing and device always returns 0 when host reads this byte.

Table 135. MR32

Addr	MR32		Thermal Sensor Critical Temperature High Limit Configuration - Low Byte Notes 1, 2, 3)
Bits	Attr	Default	Description
7:0	RW	0x50	MR32[7:0]: TS_CRIT_HIGH_LIMIT_LOW MR32 and MR33 - 16 bit thermal registers define the critical temperature high limit for thermal sensor. See Table 112

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR28 [7:0] and MR29 [7:0].
3. The Reserved bits are Read Only bits. The Host must write 0 in reserved bits when writing and device always returns 0 when host reads this byte.

Table 136. MR33

Addr	MR33		Thermal Sensor Critical Temperature High Limit Configuration- High Byte (Notes 1, 2, 3)
Bits	Attr	Default	Description
7:0	RW	0x05	MR33[7:0]: TS_CRIT_HIGH_LIMIT_HIGH MR32 and MR33 - 16 bit thermal registers define the critical temperature high limit for thermal sensor. See Table 112

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR28 [7:0] and MR29 [7:0].
3. The Reserved bits are Read Only bits. The Host must write 0 in reserved bits when writing and device always returns 0 when host reads this byte.

Table 137. MR34

Addr	MR34		Thermal Sensor Critical Temperature Low Limit Configuration- Low Byte (Notes 1, 2, 3)
Bits	Attr	Default	Description
7:0	RW	0	MR34[7:0]: TS_CRIT_LOW_LIMIT_LOW MR34 and MR35 - 16 bit thermal registers define the critical temperature low limit for thermal sensor. See Table 112

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. Critical temperature Low Limit value must have a lower value than temperature Low Limit (MR30 [7:0] and MR31 [7:0].
3. The Reserved bits are Read Only bits. The Host must write 0 in reserved bits when writing and device always returns 0 when host reads this byte.

Table 138. MR35

Addr	MR35		Thermal Sensor Critical Temperature Low Limit Configuration- High Byte (Notes 1, 2, 3)
Bits	Attr	Default	Description
7:0	RW	0	MR35[7:0]: TS_CRIT_LOW_LIMIT_HIGH MR34 and MR35 - 16 bit thermal registers define the critical temperature low limit for thermal sensor. See Table 112

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR30 [7:0] and MR31 [7:0].
3. The Reserved bits are Read Only bits. The Host must write 0 in reserved bits when writing and device always returns 0 when host reads this byte.

Table 139. MR48

Addr	MR48		Device Status
Bits	Attr	Default	Description
7	RO	0	MR48[7]: IBI_STATUS Device Event In Band Interrupt Status 0 = No pending IBI 1 = Pending IBI
6:4	RV	0	MR48[6:4]: Reserved
3	RO	0	MR48[3]: WR_OP_STATUS Write Operation Status 0 = No internal write operation is on-going; 1 = Internal write operation is on-going; Device ignores Host Write command if Host attempts to write when this bit is 1. The device self clears this bit to 0 when its completes internal write operation

Table 139. MR48 (Continued)

Addr	MR48		Device Status
Bits	Attr	Default	Description
2	RO	-	MR48[2]: WP_OVERRIDE_STATUS Write Protect Override Status 0 = Override of write protect bits in MR12 and MR13 are blocked 1 = Override of write protect bits in MR12 and MR13 are allowed The default state of this register reflects the sensing of HSA pin during power on. This bit is set to 1 if HSA pin is directly tied to GND. This bit is set to 0 if HSA pin is connected to GND through a resistor
1:0	RV	0	MR48[1:0]: Reserved

Table 140. MR49

Addr	MR49		Current Sensed Temperature - Low Byte (Notes 1, 2)
Bits	Attr	Default	Description
7:0	RO	0	MR49[7:0]: TS_SENSE_LOW MR49 and MR50 - 16 bit thermal registers return the most recent conversion of the thermal sensor See Table 112

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. The device always returns 0 from reserved bits when host reads this byte.

Table 141. MR50

Addr	MR50		Current Sensed Temperature - High Byte (Notes 1, 2)
Bits	Attr	Default	Description
7:0	RO	0	MR50[7:0]: TS_SENSE_HIGH MR49 and MR50 - 16 bit thermal registers return the most recent conversion of the thermal sensor See Table 112

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.
2. The device always returns 0 from reserved bits when host reads this byte.

Table 142. MR51

Addr	MR51		Thermal Sensor Temperature Status (Note 1)
Bits	Attr	Default	Description
7:4	RV	0	MR51[7:4]: Reserved
3	RO	0	MR51 [3:]: TS_CRIT_LOW_STATUS Temp Sensor Critical Low 0 = Temperature is above the limit set in MR34 and MR35 1 = Temperature is below the limit set in MR34 and MR35
2	RO	0	MR51[2]: TS_CRIT_HIGH_STATUS Temp Sensor Critical High 0 = Temperature is below the limit set in MR32 and MR33 1 = Temperature is above the limit set in MR32 and MR33
1	RO	0	MR51[1]: TS_LOW_STATUS Temp Sensor Low 0 = Temperature above limit set in registers MR30 and MR31 1 = Temperature below limit set in registers MR30 and MR31
0	RO	0	MR51[0]: TS_HIGH_STATUS Temp Sensor High 0 = Temperature is below the limit set in registers MR28 and MR29 1 = Temperature is above the limit set in registers MR28 and MR29

1. This entire register is only applicable if MR1 [7:0] programmed value is either 0x18 or 0x14 or 0x12.

Table 143. MR52

Addr	MR52	Default	Hub and Thermal Sensor Error Status
Bits	Attr		Description
7	RO	0	MR52[7]: BUSY_ERROR_STATUS Write or Read Attempt while SPD Device was Busy (Write Recovery Time Violation) (Notes 1, 2) 0 = No write or read attempt while SPD Hub device was busy 1 = Write or Read attempt while SPD device was busy
6	RO	0	MR52[6]: WR_NVM_BLK_ERROR_STATUS Write Attempt to Protected NVM Block 0 = No write attempt 1 = Write attempt to protected NVM Block
5	RO	0	MR52[5]: WR_NVM_PRO_REG_ERROR_STATUS Write Attempt to NVM Protection Registers 0 = No attempt to modify write protect registers 1 = Write attempt to modify write protect registers
4:2	RV	0	MR52[4:2]: Reserved
1	RO	0	MR52[1]: PEC_ERROR_STATUS Packet Error (Notes 3, 4) 0 = No PEC Error 1 = PEC Error in one or more packets
0	RO	0	MR52[0]: PAR_ERROR_STATUS Parity Check Error (Notes 4, 5) 0 = No Parity Error 1 = Parity Error in one or more bytes

1. SPD device busy status is only for accessing EEPROM memory. For any access to volatile register space, this bit definition does not apply.
2. When SPD device is busy with EEPROM write/read, it sends NACK to the host requests within write recovery time.
3. Only applicable MR18 [5] = 1 and if PEC function is enabled.
4. This register is updated to 0 when SPD5 Hub device goes through bus reset as described in Bus Reset.
5. Only applicable in MR18 [5] = 1 and if Parity function is not disabled or for supported CCC in I^2C mode.

4. Package Outline Drawing

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

5. Marking Diagram

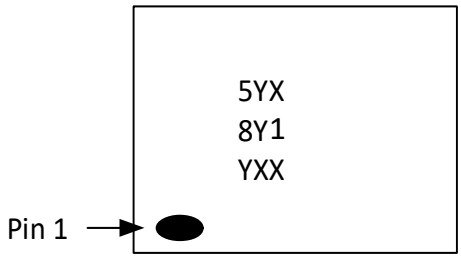


Figure 35. Top Marking

Line 1: 5; Y = Device Type Identifier (Y = 1); X = Temp Sensor Identifier (1 = with Temperature Sensor; 0 = without Temperature Sensor)

Line 2: 8 = SPD Device; Y = Mask Revision; 0 = Minor Revision

Line 3: Y = Year (9 = 2019; 0 = 2020; 1 = 2021, etc.); XX = Sequential letters for internal logistics

Black Circle Dot = Pin 1 indicator

6. Ordering Information

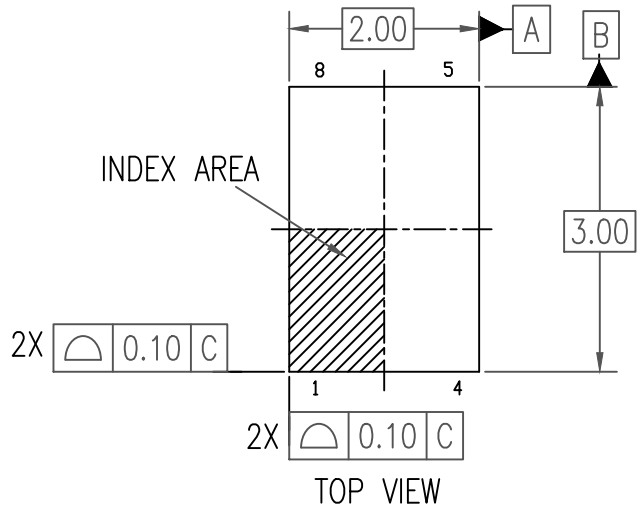
Table 144. Ordering Information

Revision	Part Number	Package	Hub Function	Temp. Sensor	Carrier Type	Temp. Range
Rev B1	SPD5118-Y1B000NCG8	2.0 × 3.0 × 0.75 mm, 8-DFN	Yes	Yes	Tape & Reel	-40 to 125°C
Rev B1	SPD5108-Y1B000NCG8		Yes	No	Tape & Reel	
Rev B1	SPD5118-Y1B000NCG		Yes	Yes	Cut Reel	
Rev B1	SPD5108-Y1B000NCG		Yes	No	Cut Reel	

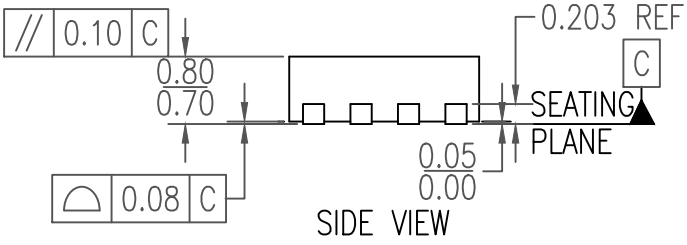
7. Revision History

Rev.	Date	Description[1]
1.11	Sep 15, 2021	Updated high/low bytes for -40°C in Thermal Register Examples table.
1.10	Aug 3, 2021	Updated Open Drain Interface with Internal On Die Pull-up Resistor
1.00	Jun 8, 2021	Initial release.

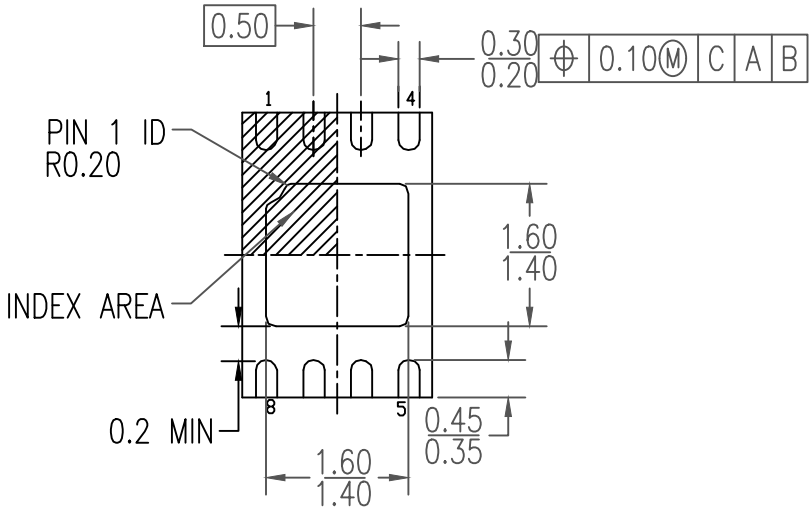
1. The parameters in this datasheet are defined in accordance with JEDEC Standard.



TOP VIEW



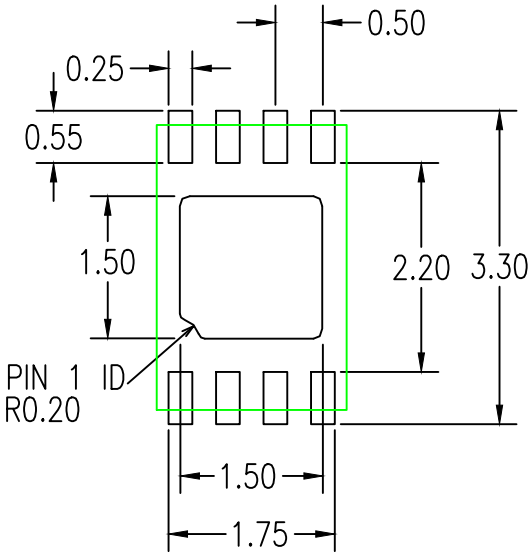
SIDE VIEW



BOTTOM VIEW

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. ALL DIMENSIONS ARE IN MILLIMIMETERS ANGLES ARE IN DEGREES
3. PIN 1 LOCATION IS EITHER IDENTIFIED BY NOTCH OR CHAMFER



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.
4. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.

Package Revision History		
Date Created	Rev No.	Description
June 26, 2018	Rev 01	Add Component Outline for Foot Print in Green
June 4, 2021	Rev 02	Update to Renesa Logo

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