High Performance Multi-mode PWM Controller

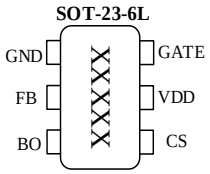
General Description

The AP8270 is a highly integrated current mode PWM control IC for high performance, low standby power and cost effective offline flyback converter applications.

QR-PWM, QR-PFM, Burst-mode operation and low consumption device help to meet the standby energy saving standards and achieve higher efficiency. Excellent EMI performance is achieved with frequency modulation.

The AP8270 offers complete protections including pin open/short protection, cycle-by-cycle current limiting, VDD over voltage protection, under voltage lockout, on-chip/external over temperature protection, output over voltage protection, over load protection, etc.

Package/Order Information



Order codes	Package
AP8270TC-A1	SOT-23-6L

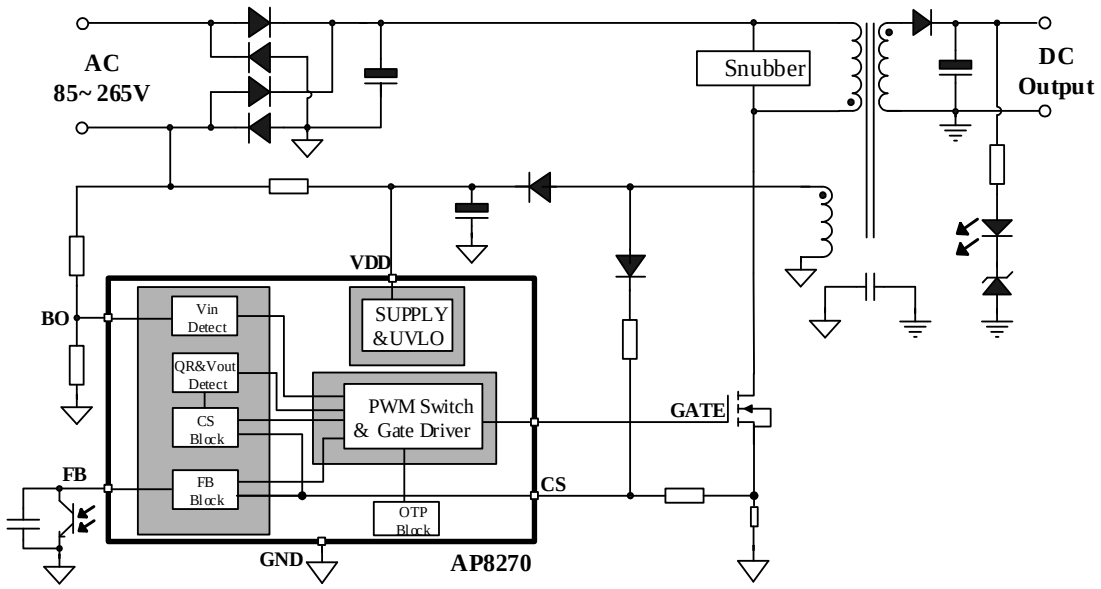
Features

- Soft Start-up Function
- Multi-mode Operation to Achieve Higher Efficiency
- Maximum Switching Frequency 120kHz
- CCM Operating Frequency 100kHz
- Internal Slope Compensation
- Internal Line Voltage Compensation
- Excellent Protection Coverage
  - ✧ Brown in/out Protection
  - ✧ VDD Over Voltage Protection
  - ✧ Output Over Voltage Protection
  - ✧ Cycle-by-Cycle Current Limiting Protection
  - ✧ Output Open/Short Protection
  - ✧ Over Load Protection
  - ✧ Over Temperature Protection

Application

- Stand-by Power
- Open-frame SMPS
- Adaptor

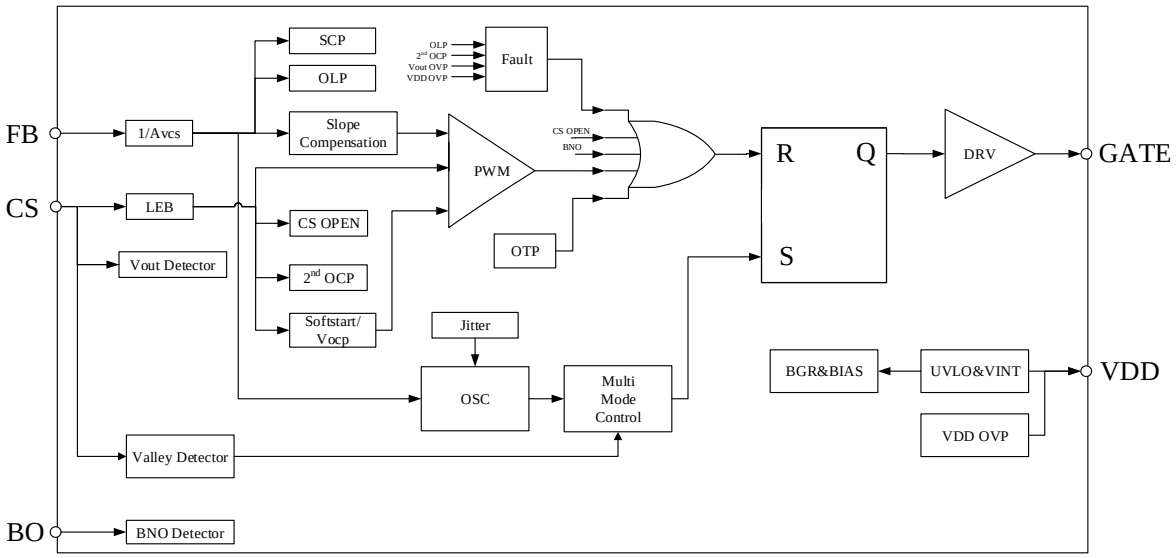
Typical Circuit



Pin Definitions

Pin Name	Pin Number	Pin Function Description
GND	1	Ground
FB	2	Feedback input pin
BO	3	Input brown in/out detection pin
CS	4	Current sense input
VDD	5	Positive supply voltage input
GATE	6	Totem-pole gate drive output for the power MOSFET.

Block Diagram



Absolute Maximum Ratings

Pin VDD……-0.3~33V
Pin FB, CS, BO……-0.3~6.5V
Pin GATE……-0.3~16V
Storage Temperature Range……-55~150℃

Lead Temperature (Soldering, 10Secs)……260℃
Package Thermal Resistance θ_{JA} (SOT-23-6L) ……160℃/W
HBM ESD Protection [1]…… ±2kV

Note：
1. Test standard: ANSI/ESDA/JEDEC JS-001-2017

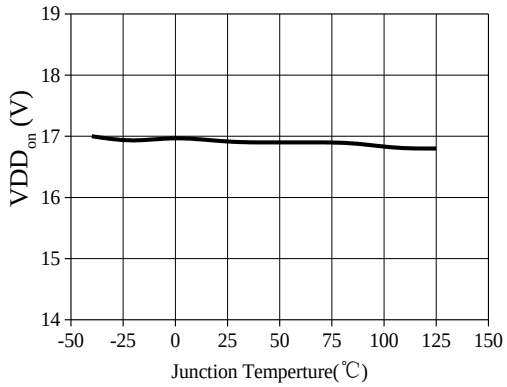
Electrical Characteristics

(T_A= 25℃, VDD=20V, unless otherwise specified)

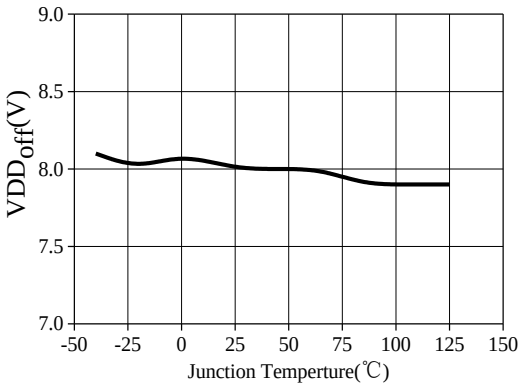
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD Supply Voltage Section						
VDD start up threshold	VDD_{on}		15.9	16.9	17.9	V
VDD under voltage shutdown threshold	VDD_{off}		7	8	9	V
VDD OVP voltage	V_{ovp}		26	28	30	V
Pull-up PMOS active	$V_{pull-up}$			10		V
VDD Supply Current Section						
Start-up charging current	I_{VDD_ST}	VDD=VDD_{on}- 1V		4	7	uA
Operating supply current, switching	I_{VDD0}	V_{FB}=3.0V,CS=0.3V	1.0	2	3	mA
Operating supply current, under burst mode	I_{VDD1}	V_{FB}=0.5V,CS=0.3V	0.4	0.8	1.5	mA
Operating supply current, with protection tripping	I_{VDD_Fault}		0.2	0.5	1.0	mA
Oscillator Section						
Maximum operating frequency	Fosc_QR			120		kHz
CCM switching frequency	F_{OSC}		95	100	105	kHz
Burst mode frequency	Fosc_BM	V_{FB}=1.5V,CS=0.3V	22	27	32	kHz
Jitter frequency	F_jitter			260		Hz
Frequency modulation range	△Fosc			±7		%
FB Section						
FB open loop voltage	V_{FB}		4.5	4.8	5.4	V
FB short current	I_{FB_SHORT}		0.15	0.20	0.25	mA
PWM input gain	A_{VCS}	$\Delta V_{FB}/\Delta V_{CS}$		3.5		V/V
Input impedance of FB	Z_{FB_IN}			25		kΩ
Maximum duty cycle	Dmax		70	80	90	%
Green mode entry voltage	V_{FB_PFM}			1.97		V
Burst mode entry voltage	$V_{FB\_BM\_L}$			1.15		V
Burst mode ending voltage	$V_{FB\_BM\_H}$			1.25		V
OLP threshold voltage	Vth_OLP			4.05		V
OLP De-Bounce time	Td_OLP			60		ms

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current Sense Section						
Soft-start time	Tss			7.5		ms
Leading edge blanking time	T_{LEB}			330		ns
Internal current limiting threshold voltage	Vth_OC		0.46	0.5	0.54	V
Internal current limiting threshold voltage	Vth_CLP			0.75		V
De-Bounce time	Td_OC			100		ms
BO Section						
Brown in threshold voltage	V_{BNI}		1.02	1.1	1.18	V
Brown out pull-up current	I_{BO}		0.5	1	2	uA
Brown out threshold voltage	V_{BNO}		0.92	1	1.08	V
Brown out protection delay time	Td_BNO			27		ms
GATE Section						
Output clamp voltage level	V_clamping		12	14	16	V
Output rising time	T_r	CL=1000pF		250		ns
Output falling time	T_f	CL=1000pF		50		ns
Thermal Section						
Thermal shutdown temperature	T_{SD}			150		℃
Thermal shutdown hysteresis	T_{HYST}			30		℃

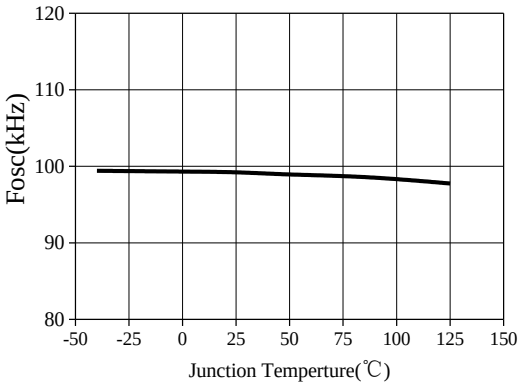
Typical Characteristics Plots



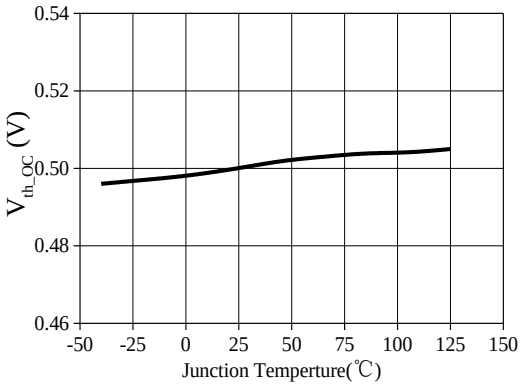
(a) VDD_{on} VS T_j



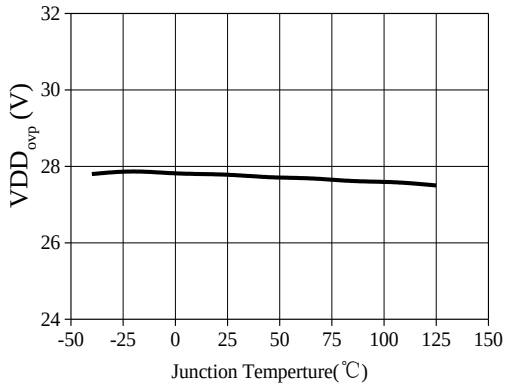
(b) VDD_{off} VS T_j



(c) F_{OSC} vs T_j



(d) V_{th_OC} VS T_j



(e) VDD_{ovp} VS T_j

Functional Description

1. Start-up

The startup current of AP8270 is designed to be very low so that VDD could be charged up above VDD_{on} threshold level and device starts up quickly. Also a large value startup resistor can be used to minimize the power loss.
When the VDD voltage reaches VDD_{on}, the chip starts to work. After the start-up process, the auxiliary winding of the transformer provides energy to the VDD capacitor.

2. Soft Start-up

In the process of start-up, the current of drain increases to maximum limitation step by step. As a result, it can reduce the stress of secondary diode greatly and prevent the transformer turning into the saturation state. Typically, the duration of soft-start is 7.5ms.

3. Quasi-Resonant Switching

The valley detection is realized by CS pin. High conversion efficiency is achieved with quasi-resonant mode. The operating frequency is determined by the transformer parameters during PWM operation. The maximum operating frequency is limited to 120kHz. As the load increases or the input voltage decreases, the operating frequency of AP8270 will reduced and the switching frequency will be fixed at 100kHz during CCM operation.

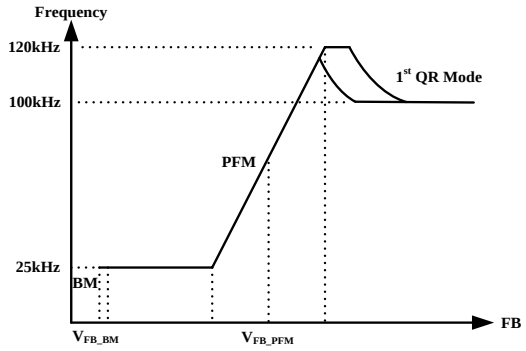


Fig.1 Curve diagram of FB and frequency

4. PFM Mode

PFM operation helps to meet the standby energy saving standards and achieve higher efficiency. When FB is less than V_{FB_PFM}, AP8270 enters PFM Mode. The lighter the load, the lower the switching frequency will reduce continuously as the load reduces. The switching frequency will fixed at 25kHz as it reaches the minimum switching frequency.

5. Burst-mode Operation

AP8270 enters burst-mode operation in order to minimize the power dissipation in standby mode. As the load decreases, the feedback voltage decreases. When the voltage on FB pin falls below $V_{FB\_BM\_L}$, the device enters burst mode and power MOSFET stops switching. It can be switched on again once the voltage on FB pin exceeds $V_{FB\_BM\_H}$.

6. Gate Driver

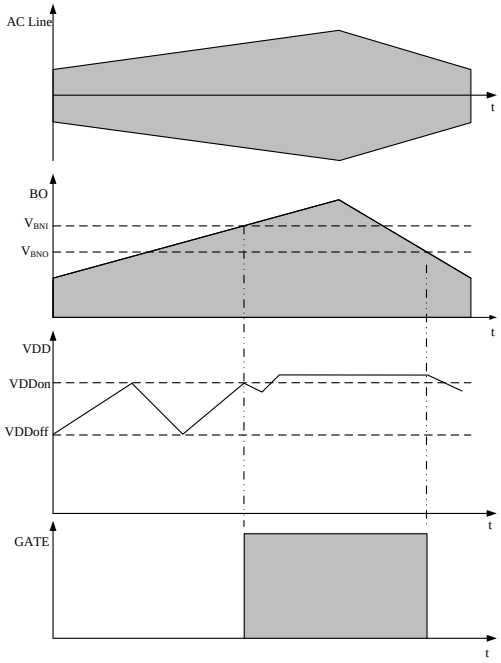
The output stage of AP8270 is a fast totem pole gate driver. Dead time has been added to minimize heat dissipation, increases efficiency and enhances reliability. The output driver is clamped by an internal 14V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

7. Output Over-Voltage Protection

AP8270 realizes precise over-voltage protection by sampling the auxiliary winding voltage through CS pin during the demagnetization stage. When the sampled CS voltage is greater than 0.3V and lasts for 7 successive PWM cycles, the output OVP protection is triggered and the gate driver is turned off. The output OVP protection point can be set by selecting an appropriate resistance value.

8. Input Brown Out Protection

The brown in/out function of AP8270 is realized by judging the sampled voltage of BO pin. The brown in/out protection threshold can be set by adjusting the resistance value of the upper and lower bias resistance. When the sampled voltage of BO pin is less than the VBNI, the output gate is off; During VDD start-up stage, when the sampled voltage of BO pin exceeds VBNI, the gate of AP8270 starts operating. Once the operation starts, the voltage of BO pin is continuously detected. If the detected voltage is less than VBNO for a time of Td_BNO, the brown out protection is triggered and the gate is off.



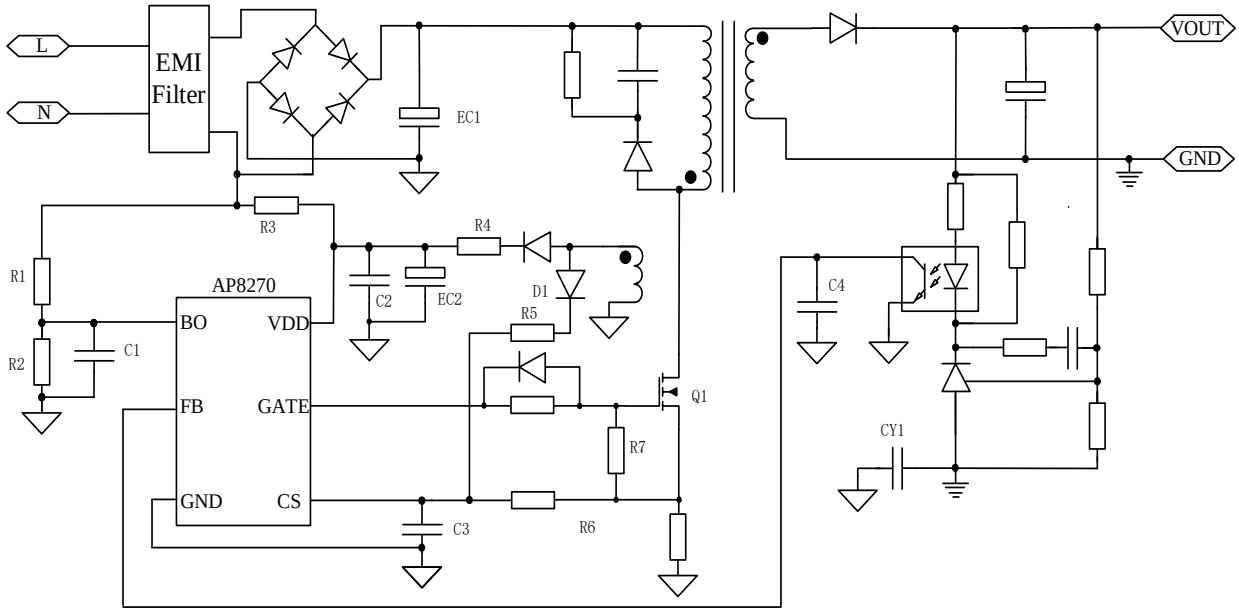
9. Over Load Protection (OLP)

Overload is defined as the load current exceeding a pre-set level due to an accident event as a fault. If FB exceeds Vth_OLP for more than Td_OLP (de-bounce time of OLP), the protection circuit should be activated to protect the SMPS.

10. Over Temperature Protection

Both an internal OTP circuit and an external OTP circuit are embedded inside the AP8270 to prevent the system from hot damage. If the temperature exceeds about 150℃.

Typical Application

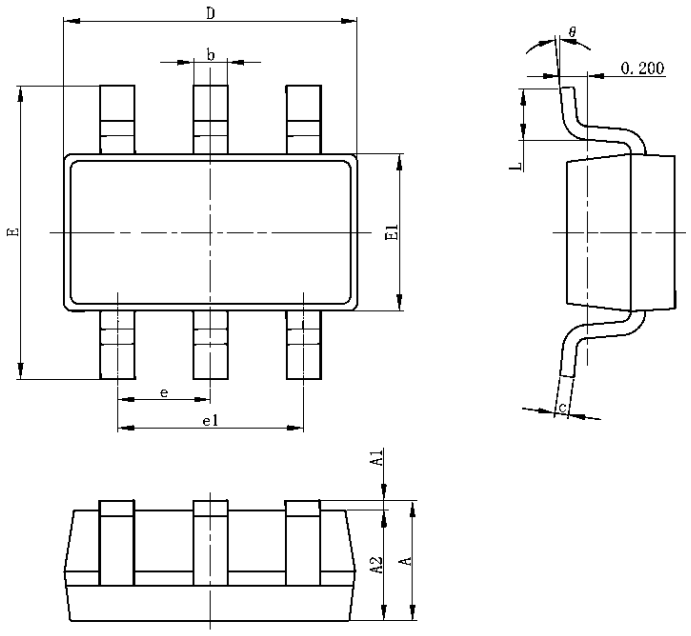


Component Parameter and Layout Considerations:

1. It is recommended to use two or more 1206 in series for starting resistor R3 and connect it directly to the front end of rectifier bridge. If EC2 selects 10uF, it is recommended that R3 should not be greater than 660kΩ.
2. VDD electrolytic EC2 shall be placed closest to VDD pin and GND pin. It is recommended to reserve another ceramic capacitor C2 near VDD pin with a capacity of 100nF
3. It is recommended that a current limiting resistor with a recommended value of 6.8Ω added in serial in the auxiliary coil supply circuit.
4. The lower resistor R2 and the ceramic capacitor C1 should be placed closely to the BO pin and GND pin. It is recommended to use 47kΩ for R2 and 1nF for C1; it is recommended that two or more 1206 resistors be connected in series to the upper resistor R1 and directly to the front end of the rectifier bridge. The value of R1 shall be selected according to the AC brown in/out protection point.
5. It is recommended to select 330Ω for R6, and the resistance value of R5 shall be selected according to the overvoltage protection point of output voltage; At the same time, the filter capacitor C3 is recommended to be 100pF and placed as close to the CS pin as possible; In addition, D1 suggests to use fast pipe, such as FR107.
6. The capacitance of C4 is recommended to be 1nF, and placed closely to the FB pin.
7. In application, it is generally recommended to connect a resistor R7 in parallel between the GS close to the power MOS, and the recommended resistance value is 10kΩ.

Package Information

Package Information SOT-23-6L



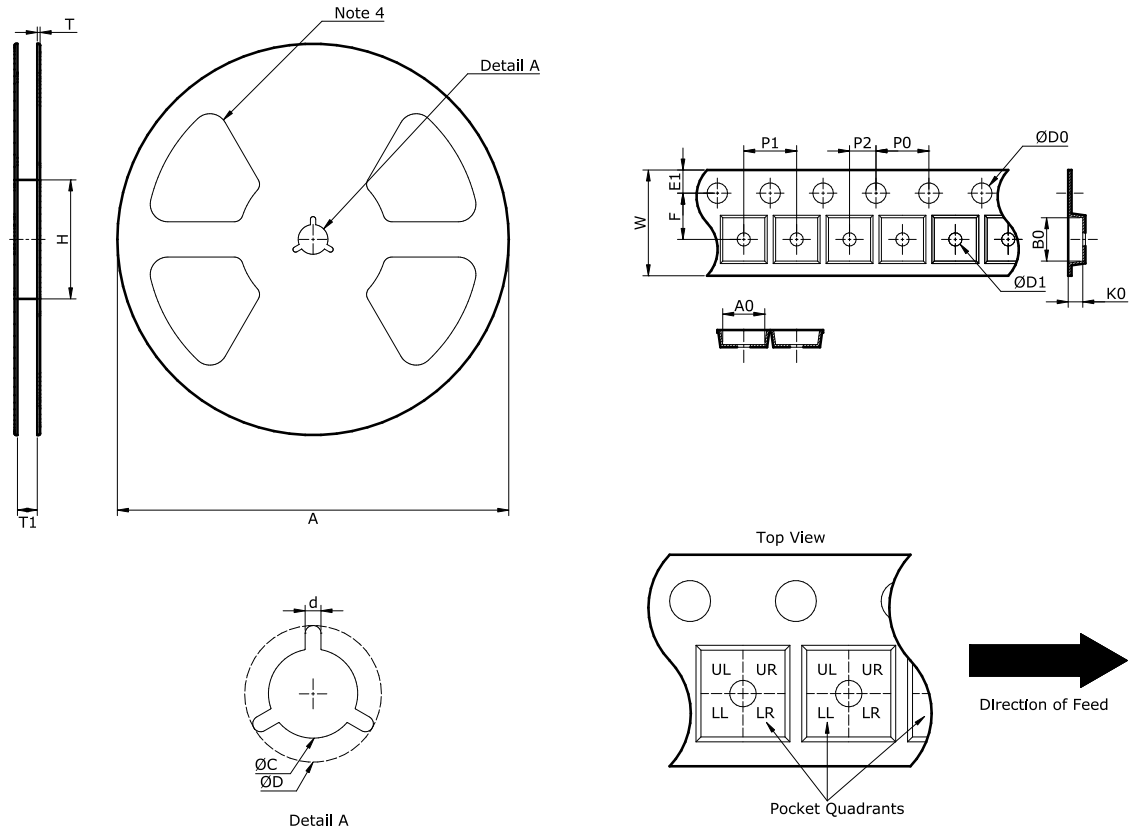
Symbol \ Size	Min. (mm)	Max. (mm)	Symbol \ Size	Min. (mm)	Max. (mm)
A	1.050	1.250	E1	1.500	1.700
A1	0.000	0.100	E	2.650	2.950
A2	1.050	1.150	e	0.950(BSC)	
b	0.300	0.500	e1	1.800	2.000
c	0.100	0.200	L1	0.300	0.600
D	2.820	3.020	Θ	0 º	8 º

Order codes	Top mark	Package
AP8270	70YWL	SOT-23-6L

Note: Y: Year code; W: Internal code; L: Batch code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Tape and Reel Information



SOT-23-6L Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
180 +0/-3	1.4 ±0.3	9.5 ±1.0	60 ±0.5	13.00 ±0.20	18.70 ±0.40	2.30 ±0.10	3.17 ±0.10	3.10 ±0.1	1.10 ±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
8.0 +0.3/-0.1	3.5 ±0.1	1.75 ±0.1	4.0 ±0.10	4.0 ±0.1	2.0 ±0.05	1.5 +0.1/-0	1.0 +0.25/-0	LL	

Notes:
1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

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